ELECTRICAL PERFORMANCE CHARACTERISTICS OF HIGH POWER CONVERTERS FOR SPACE POWER APPLICATIONS

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FOREWORD

This report presents the results of NASA Grant NAG-3-708, "Electrical Performance Characteristics of High Power Converters for Space Power Applications," for the period of January 1, 1988 to September 30, 1989. This research was performed by The University of Toledo for the NASA Lewis Research Center.

TABLE OF CONTENTS

I. INTRODUCTION

The purpose of this research was to study various electric transmission and distribution (T&D) systems that would be suitable for nuclear powered spacecraft. Both DC and 20 kHz systems were considered, and Fig. I-1 shows the block diagram of a system that could be adapted to either of these alternatives. For 20 kHz operation, the system would be identical to that in Fig. I-1. In this case, the source converter and the fixed frequency Schwarz converter are connected in cascade to produce 20 kHz. The resulting output waveform will be trapezoidal in shape, as described in [5,9-13,17]. A DC system can be achieved simply by removing the Schwarz converter.

These systems are expected to operate at power levels in excess of 100 kw and at rather low input voltages, e.g., 100 Vdc. The system in Fig. I-1 uses a thermoelectric converter to transform heat from the nuclear reactor to electric energy. To reduce the amount of radiation shielding and thus weight, it is assumed that the nuclear reactor and thermoelectric converter will be located on an extension arm away from the spacecraft. Since the typical source current will exceed 1000 Adc, it is also desirable to place an electronic converter near the reactor to increase the voltage and thus decrease cable weight. The system in Fig. I-1 also includes another converter for controlling the power to a ballast load. This is used to maintain a constant load on the reactor as the spacecraft load varies.

Locating converters near the reactor creates other problems however, because of the high temperature and radiation environment created by the reactor. Because of the relatively high weight of the heat radiators, there is a strong incentive to operate these converters at a relatively high temperature. This implies that forced commutated converters should be used since the polypropolene capacitors often used in resonant designs are limited to about 85°C.

The relationship between surface area and temperature of a radiator is provided by Stefan's law,

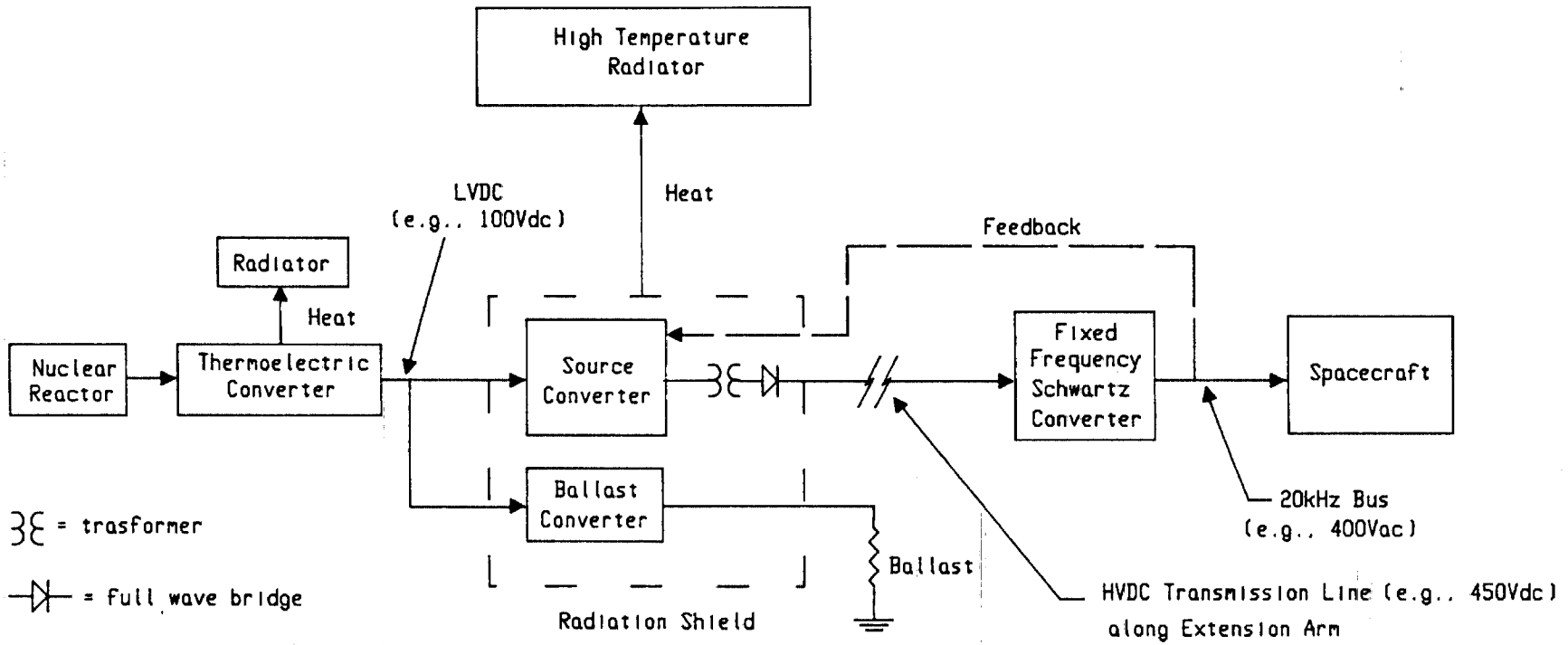


Fig I-1. Electric power system driven by a nuclear reactor.

$$Q = \varepsilon\sigma\gamma A\left(T^4 - T_s^4\right)$$

where Q = rate of emission of radiant energy (watts)

ε = emissivity of the surface (e.g., about 0.3 for Cu)

$\sigma = 5.6699 \times 10^{-8}$ in SI units

γ = configuration factor

A= radiator surface area

T = radiator temperature (°K)

Ts= sink temperature (assumed to be 273°K)

For an 85°C system,

$T \equiv T_L = 85°C + 273°C = 358°K$

$\therefore\ Q_L = \varepsilon\sigma\gamma A_L\left(358^4 - 273^4\right)$

And for a 120°C system,

$T \equiv T_H = 120°C + 273°C = 397°K$

$\therefore\ Q_H = \varepsilon\sigma\gamma A_H\left(397^4 - 273^4\right).$

Assuming that Q and γ are the same for both systems,

$Q_L = Q_H$

$\therefore\ A_L\left(1.087 \times 10^{10}\right) = A_H\left(1.929 \times 10^{10}\right)$

$\therefore\ A_L = 1.77\ A_H$

This indicates that the 85°C radiator would require 77% more surface area than the 120°C radiator.

Bipolar power transistors with T_{Jmax} = 200°C such as the Westinghouse D62T or D7ST, conceivably could be operated with heat sink temperatures of 120°C and still process a significant amount of power. Likewise, other circuit components such as magnetics, filter capacitors, and control circuits also can be operated in the

120°C range. Thus, the resonant capacitor appears to be the device that will limit the maximum operating temperature of a resonant converter, and this motivates the consideration of force commutated converters. These circuits may have higher losses, but it is conceivable that they could be operated at higher temperatures to decrease radiator weight and thus decrease total system weight.

Once it was decided to use force commutated (i.e., PWM) converters, the next question was to determine which topology. Various topologies were considered for the source converter in Fig. I-1, but the final choice was between the following two:

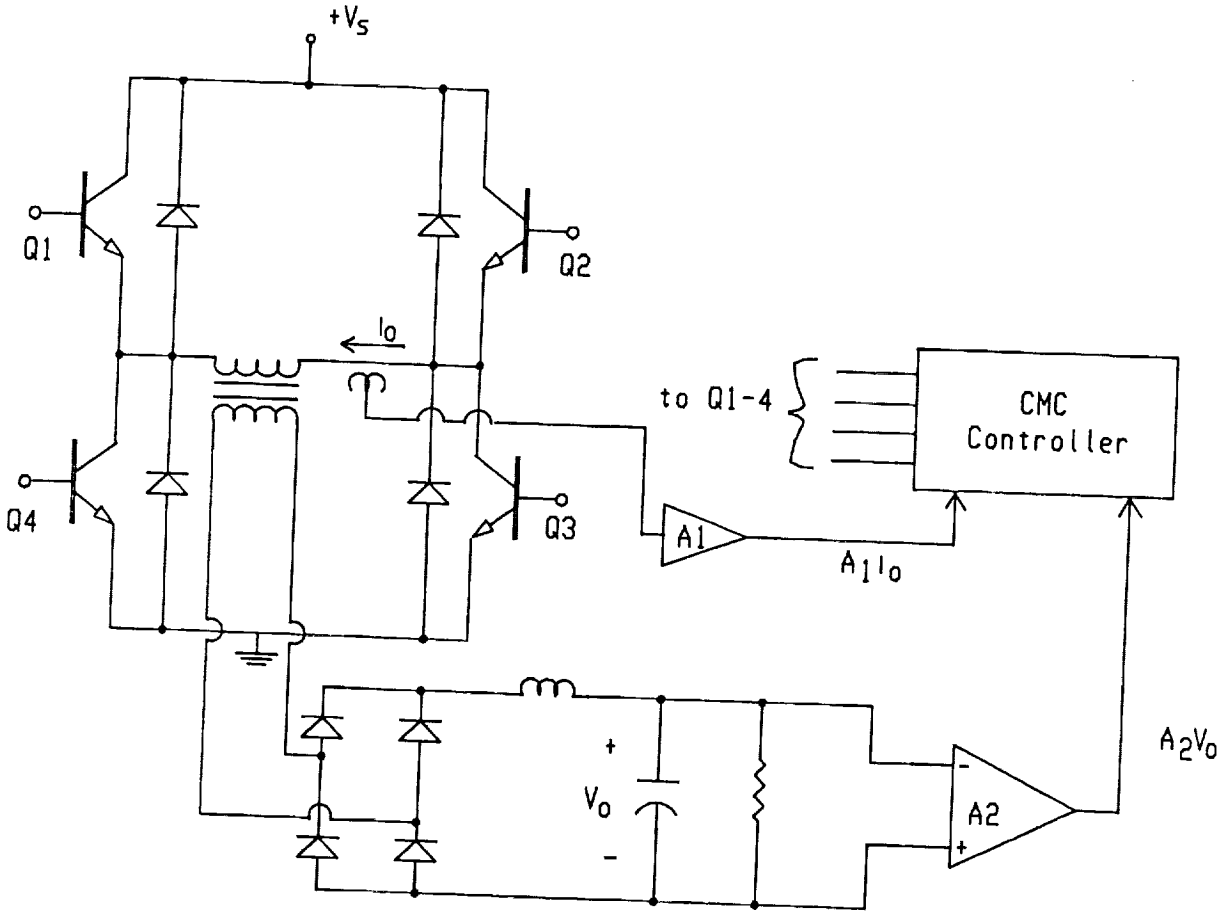
1. Full bridge with current mode control (CCM) in Fig. I-2. CCM is needed with a full bridge to prevent transformer saturation due to flux imbalance.

2. Push-pull current-fed (PPCF) in Fig. I-3.

PPCF requires higher transistor voltages, but it uses a much less complex control circuit. (Part of the complexity of CMC results because its controller needs a very accurate, noise-free replica of the instantaneous current waveform.) PPCF also can be designed to deliver full output voltage at half power when the input voltage decreases by 50%. This last option was considered to be important because of the possibility of a short circuit across half of the thermoelectric converter which would remove half of the input voltage. Because of its relative simplicity and the half power option, it was decided to use the PPCF topology. The higher transistor voltage was not considered to be a serious problem because of the relatively low input voltage in the 100 Vdc range.

The design of the ballast converter, which is controlled to operate as a shunt regulator, was also investigated. Only designs capable of 120°C operation were considered. Automatic redundancy was considered a useful option, and this feature was explored in the shunt regulator design. Appropriate static and dynamic models were developed and confirmed experimentally with a 2500-W 20-kHz shunt regulator and a simulated thermoelectric converter.

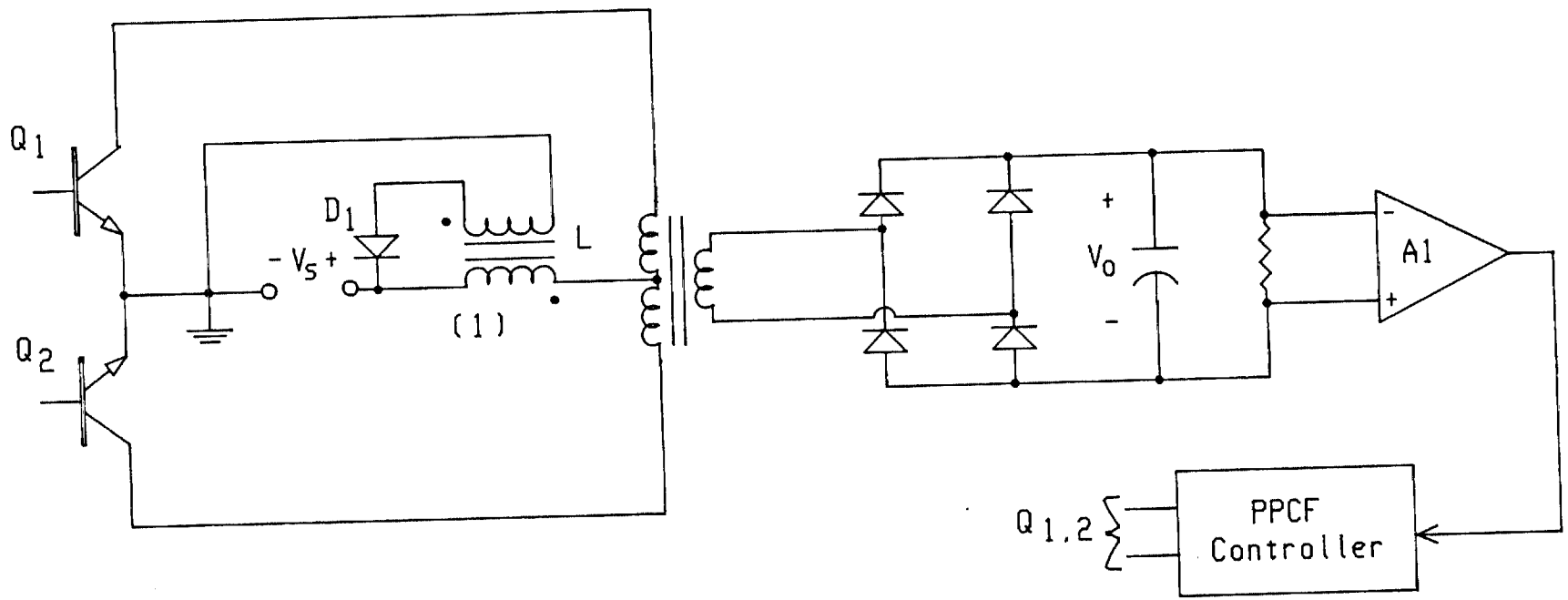
A typical thermoelectric converter is known to have a high internal resistance. Because of the negative input resistance of the regulated source converter, there is a possible bistable mode of operation for the system should the



A_1= Instantaneous current sensor

A_2= average voltage sensor

Fig. I-2. Full bridge converter with current mode control (CMC).



(1) The secondary of L also can be connected across the output, but this requires much higher voltage ratings for D1 if Vo >> Vs..

A1=average voltage sensor

Fig.I-3. Push-pull current-fed converter.

shunt regulator ever drop out. Simulation and experiment confirmed that a momentary overload on the system could trigger an unfavorable operating point. A simple preventative measure was found, however.

A final report is also presented on the experimental performance of the 2500 W phase-controlled parallel-loaded resonant inverter described in the previous report on this grant. Full-power fault-tolerant operation was obtained. Details of the experimental setup used are presented along with scope photos showing the short-circuit transient and its effect on the inverter.

II. OPEN LOOP TRANSFER FUNCTIONS FOR THE PUSH-PULL CURRENT-FED CONVERTER

Although the topology of the PPCF configuration in Fig. II-1 was first reported several years ago [2-4], it appears that the equation for the small signal open loop gain has never been published. If the secondary of L is connected to the output instead of the input, the open loop gain will be the same as that of a conventional buck regulator. This is not the case with the present circuit in Fig. II-1 however, so it was necessary to derive this equation in order to stabilize the loop in an objective manner.

Voltage Regulation Loop

Fig. II-1 shows a simplified schematic of the PPCF converter in the voltage regulation mode. The open loop transfer function can be derived using the state space averaging and linearization procedure [14.]. The differential equations for the two conduction intervals are as follows,

Interval #1: $o \le t \le d_1 T$

$$\dot{x}_1 = -\frac{x_2}{L} + \frac{V_1}{L} \qquad (II\text{-}1)$$

$$\dot{x}_2 = \frac{x_1}{C} - \frac{x_2}{RC} \qquad (II\text{-}2)$$

$$\text{or} \quad \dot{\underline{x}} = A_1 \underline{x} + B_1 V_1 \qquad (II\text{-}3)$$

$$\text{where} \quad A_1 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \qquad (II\text{-}4)$$

$$B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \qquad (II\text{-}5)$$

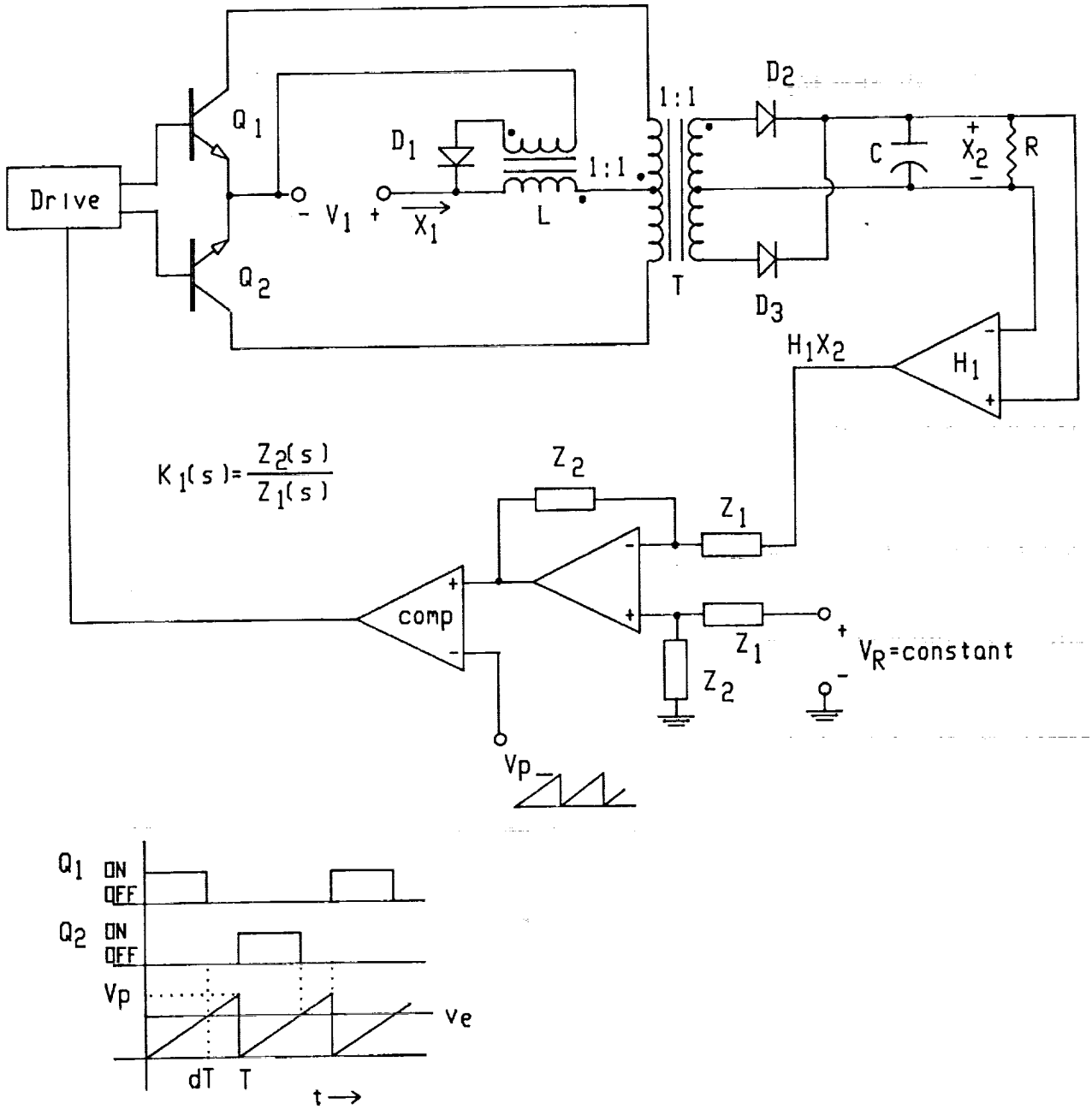


Fig.Ⅱ-1. PWM control for PPCF converter in the voltage regulation mode.

Interval #2: $d_1T \le t \le T$

$$\dot{x}_1 = -\frac{V_1}{L} \qquad \text{(II-6)}$$

$$\dot{x}_2 = -\frac{x_2}{RC} \qquad \text{(II-7)}$$

or $$\dot{\underline{x}} = A_2 \underline{x} + B_2 V_1 \qquad \text{(II-8)}$$

where $$A_2 = \begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{RC} \end{bmatrix} \qquad \text{(II-9)}$$

$$B_2 = \begin{bmatrix} \frac{-1}{L} \\ 0 \end{bmatrix} \qquad \text{(II-10)}$$

We can write the following approximate derivatives if the switching frequency is high with respect to the natural frequencies of the circuit and any signal frequencies,

$$\dot{\underline{x}}_{(0)} = \frac{\underline{x}(d_1T) - \underline{x}(0)}{d_1T} \qquad \text{(II-11)}$$

$$\dot{\underline{x}}(d_1T) = \frac{\underline{x}(T) - \underline{x}(d_1T)}{(1-d_1T)} \qquad \text{(II-12)}$$

From the previous equations we have,

$$\underline{x}(d_1T) = \underline{x}(0) + d_1T(A_1 \underline{x}(0) + B_1V_1 \qquad \text{(II-13)}$$

$$\underline{x}(T) = \underline{x}(d_1T) + T(1-d_1)(A_2 \underline{x}(d_1T) + B_2V_1) \qquad \text{(II-14)}$$

Substituting (II-13) into (II-14),

$$\underline{x}(T) = [\underline{x}(0)(1 + d_1TA_1) + d_1TB_1V_1][1 + T(1-d_1)A_2] + T(1-d_1)B_2V_1 \qquad \text{(II-15)}$$

Re-arranging (II-15),

$$\frac{\underline{x}(T) - \underline{x}(0)}{T} = \underline{x}(0)\,[(1 - d_1)\,A_2 + d_1A_1 + d_1A_1\,(1-d_1)\,A_2T] + V_1\,[d_1B_1 + d_1B_1\,(1-d_1)\,A_2\,T + (1-d_1)B_2] \qquad \text{(II-16)}$$

Assuming that a high switching frequency is equivalent to taking the limit of (II-16) as $T \to 0$,

$$\lim_{T\to 0}\left(\frac{x(T) - x(0)}{T}\right) = \dot{\underline{x}} = [d_1A_1 + (1 - d_1)\,A_2]\,\underline{x} + [d_1B_1 + (1 - d_1)B_2]\,V_1 \qquad \text{(II-17)}$$

In order to linearize (II-17), we need to separate the dc part of $\underline{x}$ and d_1 from the ac part,

$$\underline{x} \equiv \underline{x}_0 + \hat{\underline{x}} \qquad \text{(II-18)}$$

$$d_1 \equiv D_1 + \hat{d}_1 \qquad \text{(II-19)}$$

where $\underline{x}_o$ and D_1 are the dc components and $\hat{\underline{x}}$ and $\hat{d}_1$ are the ac components. Substituting (II-18) and (II-19) into (II-17) yields the dc equation,

$$\underline{0} = [A_1D_1 + A_2\,(1 - D_1)]\,\underline{x}_0 + [B_1D_1 + B_2(1 - D_1)]\,V_1 \qquad \text{(II-20)}$$

and the ac equation,

$$\dot{\hat{\underline{x}}} = [A_1D_1 + A_2(1-D_1)]\,\hat{\underline{x}} + [(A_1 - A_2)\,\underline{x}_0 + (B_1 - B_2)\,V_1]\hat{d}_1 \qquad \text{(II-21)}$$

where it is assumed that all products of ac terms are negligible.
Defining,

$$A_0 \equiv A_1D_1 + A_2\,(1 - D_1) \qquad \text{(II-22)}$$

$$B_0 \equiv B_1D_1 + B_2\,(1 - D_1) \qquad \text{(II-23)}$$

$$E \equiv (A_1 - A_2)\,\underline{x}_o + (B_1 - B_2)\,V_1 \qquad \text{(II-24)}$$

Therefore,

$$\underline{0} = A_o \underline{x}o + B_o V_1 \qquad \text{(II-25)}$$

$$\dot{\hat{\underline{x}}} = A_0 \hat{\underline{x}} + E \hat{d}_1 \qquad \text{(II-26)}$$

Substituting (II-4) and (II-9) into (II-22),

$$A_0 = \begin{bmatrix} 0 & -\frac{D}{L} \\ \frac{D}{C} & -\frac{1}{RC} \end{bmatrix} \qquad \text{(II-27)}$$

and (II-5) and (II-10) into (II-23),

$$B_0 = \begin{bmatrix} \frac{2D_1-1}{L} \\ 0 \end{bmatrix} \qquad \text{(II-28)}$$

and(II-4), (II-5), (II-9) and (II-10) into (II-24),

$$E = \begin{bmatrix} -\frac{x_{20}}{L} + \frac{2V_1}{L} \\ \frac{x_{10}}{C} \end{bmatrix} \qquad \text{(II-29)}$$

Current Regulation Loop

We now need to find the relationships between V_1, x_{10}, x_{20} and D_1 for the current regulation mode. The equivalent circuit for $o \le t \le d_1 T$ is shown in Fig. II-2 (a) and for $d_1 T \le t \le T$ in Fig. II-2 (b). If x_1 is continuous, the changes in the flux linkage of L, $\Delta\lambda$, during the on and off periods are,

$$\Delta\lambda on = (V_1 - x_{20}) D_1 T \qquad \text{(II-30)}$$

$$\Delta\lambda off = -V_1 (1 - D_1) T \qquad \text{(II-31)}$$

since λ remains bounded, it is necessary that,

$$\Delta\lambda on + \Delta\lambda off = 0 \qquad \text{(II-32)}$$

$$\therefore (V_1 - x_{20}) D_1 T - V_1 (1 - D_1) T = 0 \qquad \text{(II-33)}$$

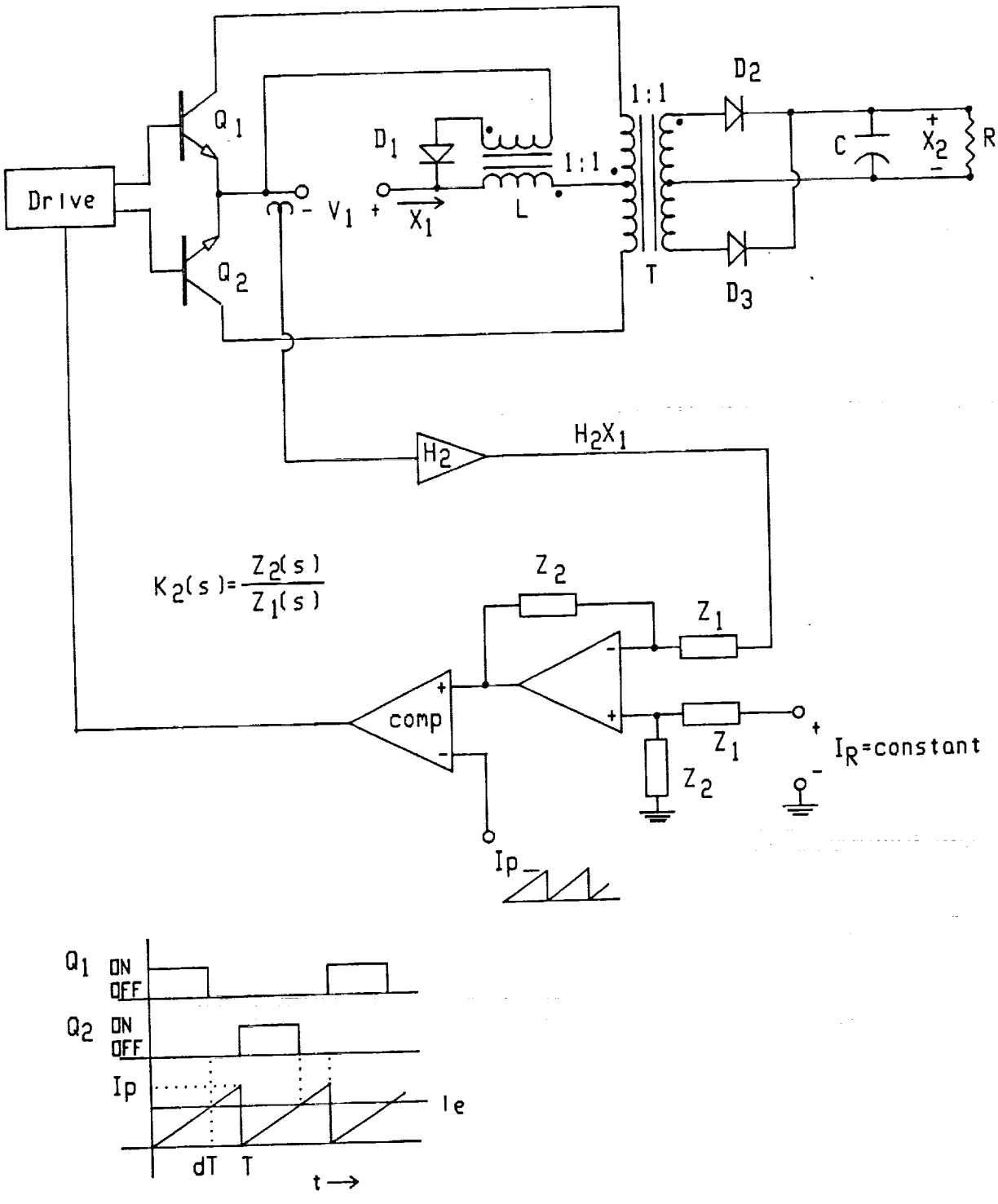


Fig. II-2. PWM control for PPCF converter in the current regulation mode.

$$x_{20} = V_1 \left(\frac{2 D_1 - 1}{D_1} \right) \qquad \text{(II-34)}$$

($D_1 > .5$ since $D_1 < .5$ means that x_1 would be discontinuous). If $P_{IN} = P_{OUT}$ represent the average input and output power,

$$P_{IN} = V_1 x_{10} D_1 - V_1 x_{10} (1-D_1) = V_1 x_{10} (2D_1-1) \qquad \text{(II-35)}$$

$$P_{OUT} = \frac{x_{20}^2}{R} = \frac{V_1^2}{R} \left(\frac{2D_1 - 1}{D_1} \right)^2 \qquad \text{(II-36)}$$

And if losses are ignored,

$$P_{IN} = P_{OUT} \qquad \text{(II-37)}$$

which yields,

$$x_{10} = \frac{V_1 (2 D_1 - 1)}{D_1^2 R} \qquad \text{(II-38)}$$

Substituting (II-34) and (II-38) into (II-29),

$$E = \begin{bmatrix} \frac{V_1}{D_1 L} \\ \frac{V_1 (2 D_1 - 1)}{D_1^2 RC} \end{bmatrix} \qquad \text{(II-39)}$$

Taking the Laplace transform of (II-26),

$$\hat{\underline{x}}_{(s)} = (SI - A_0)^{-1} E \hat{d}_{1(s)} \qquad \text{(II-40)}$$

We know that $\hat{d}_{1(s)}$ will depend on $\hat{x}_{2(s)}$ because of the voltage feedback loop. After linearization, we can express the general control law in the following form,

$$\hat{d}_{1(s)} = F_{(S)}^T \hat{x}_{(s)} \qquad \text{(II-41)}$$

From Fig. II-1 we have,

$$d_1 = \frac{v_e}{V_P} \tag{II-42}$$

Taking the Laplace transform,

$$d_{1\,(s)} = \frac{V_{e\,(s)}}{V_P} = \frac{K_{1\,(s)}V_R - K_{1\,(s)}H_1 x_{2\,(s)}}{V_P} \tag{II-43}$$

Therefore, for the time varying part, $\hat{d}_1$,

$$\hat{d}_{1\,(s)} = \frac{-K_{1\,(s)}H_1}{V_P}\,\hat{x}_{2\,(s)} \tag{II-44}$$

$$\therefore\ F^T_{(s)} = \begin{bmatrix} 0 & \dfrac{-K_{1\,(s)}H_1}{V_P} \end{bmatrix} \tag{II-45}$$

We now wish to open the control loop mathematically be replacing $\underline{\hat{x}}(s)$ in (II-41) with an independent vector $\underline{\hat{u}}(s)$. Thus,

$$\hat{d}_{1\,(s)} = F^T_{(s)}\,\underline{\hat{u}}(s) \tag{II-46}$$

and from (II-40) and (II-46),

$$\underline{\hat{x}}(s) = (sI - A_0)^{-1}EF^T_{(s)}\,\underline{\hat{u}}(s) \tag{II-47}$$

Therefore, the general ac open loop transfer function matrix, $T_{xu(s)}$, is,

$$\underline{T}_{xu(s)} \equiv (sI - A_0)^{-1}EF^T_{(s)} \tag{II-48}$$

From (II-39) and (II-45),

$$EF^T_{(s)} = \begin{bmatrix} 0 & \dfrac{-V_1K_{1(s)}H_1}{D_1LV_P} \\ 0 & \dfrac{-V_1(2D_1 - 1)K_{1(s)}H_1}{D_1{}^2RC\,V_P} \end{bmatrix} \tag{II-49}$$

Now,

$$(sI - A_0)^{-1} = \frac{1}{s^2 + \dfrac{s}{RC} + \dfrac{D_1{}^2}{LC}} \begin{bmatrix} \left(s + \dfrac{1}{RC}\right) & \dfrac{-D_1}{L} \\ \dfrac{D_1}{C} & s \end{bmatrix} \tag{II-50}$$

Substituting (II-49) and (II-50) into (II-48) yields,

$$T_{xu\,(s)} = \frac{\begin{bmatrix} 0 & \left(-\dfrac{V_1 K_{1\,(s)} H_1}{D_1 L V_P}\left(s + \dfrac{1}{RC}\right) + \dfrac{V_1\,(2\,D_1 - 1)\,K_{1\,(s)} H_1}{D_1 RLC\,V_P}\right) \\ 0 & -\left(\dfrac{V_1 K_{1\,(s)} H_1}{LCV_P} + \dfrac{V_1 (2\,D_1 - 1)\,s\,K_{1\,(s)} H_1}{D_1{}^2 RCV_P}\right) \end{bmatrix}}{s^2 + \dfrac{s}{RC} + \dfrac{D_1{}^2}{LC}} \qquad \text{(II-51)}$$

From (II-51) the small signal open loop voltage gain transfer function is,

$$G_{(s)}H_{(s)v} = -T_{xu(s)22} = \frac{V_1 K_{1(s)} H_1 \left[1 + s\,\dfrac{(2D_1 - 1)L}{D_1{}^2 R}\right]}{V_P D_1{}^2 \left[\dfrac{s^2 LC}{D_1{}^2} + \dfrac{Ls}{RD_1{}^2} + 1\right]} \qquad \text{(II-52)}$$

For the current regulation mode, (II-1) - (II-41) still apply except the duty ratio will be designated d_2 instead of d_1. From Fig. II-2 we have,

$$d_2 = \frac{i_e}{I_P} \qquad \text{(II-53)}$$

Taking the Laplace transform,

$$d_{2\,(s)} = \frac{I_{e\,(s)}}{I_P} = \frac{K_{2\,(s)}\,I_R - K_{2\,(s)} H_2 X_{1\,(s)}}{I_P} \qquad \text{(II-54)}$$

Therefore for the ac part, $\hat{d}_2$,

$$\hat{d}_{2\,(s)} = \frac{-\,K_{2\,(s)} H_2 \hat{X}_{1\,(s)}}{I_P} \qquad \text{(II-55)}$$

$$\therefore\ F^T_{(s)} = \begin{bmatrix} -\dfrac{K_{2\,(s)} H_2}{I_P} & 0 \end{bmatrix} \qquad \text{(II-56)}$$

From (II-39) and (II-56),

$$EF_{(s)}^{T} = \begin{bmatrix} \dfrac{-V_1 K_{2(s)} H_2}{D_2 L\, I_P} & 0 \\ \dfrac{-V_1(2D_2 - 1)K_{2(s)} H_2}{D_2^2 RC\, I_P} & 0 \end{bmatrix} \qquad \text{(II-57)}$$

Substituting (II-50) and (II-57) into (II-48) yields,

$$T_{xu}(s) = \frac{\begin{bmatrix} \left[\dfrac{-\left(s + \dfrac{1}{RC}\right) V_1 K_{2(s)} H_2}{D_2 L\, I_P} + \dfrac{V_1(2D_2 - 1)K_{2(s)} H_2}{D_2 RLC\, I_P}\right] & 0 \\ \left[-\dfrac{V_1 K_{2(s)} H_2}{LC\, I_P} - \dfrac{V_1(2D_2 - 1)K_{2(s)} H_2 s}{D_2^2 RC\, I_P}\right] & 0 \end{bmatrix}}{s^2 + \dfrac{s}{RC} + \dfrac{D_2^2}{LC}} \qquad \text{(II-58)}$$

From (II-58) the small signal open loop current gain transfer function is,

$$G_{(s)}H_{(s)I} = -T_{xu(s)11} = \frac{2(1 - D_2)K_{2(s)} H_2 V_1}{D_2^3 R\, I_P} \frac{\left[1 + s\left(\dfrac{RC}{2(1 - D_2)}\right)\right]}{\left[\dfrac{s^2 LC}{D_2^2} + \dfrac{Ls}{RD_2^2} + 1\right]} \qquad \text{(II-59)}$$

Discussion

An interesting result from (II-52) and (II-59) is the fact that both uncompensated open loop transfer functions have a zero that offers the possibility of canceling one of the poles. This has some similarity to current mode control (CMC) which uses a zero to compensate for one of the poles and thus extends the bandwidth [14.]. However, it remains to be seen if the zeros in (II-52) and (II-59) can be utilized to stabilize the regulator since they vary with R.

To investigate the effect of the zero in (II-52) and (II-59), the following calculations were performed for a PPCF converter with the following parameters: Frequency = 10kHz, transformer turns ratio = 1:4.87, inductor turns ratio = 1:1, L=1.215 mH, C = 0.22μfd

Case 1:

R = 205Ω , D = .73

L reflected to transformer secondary = $L' = (4.87)^2(1.215) = 28.8$ mH

$\frac{LC}{D^2} = 1.19 \times 10^{-8}$, $\frac{L}{RD^2} = .26 \times 10^{-3}$

$\therefore$ poles $= 16.84 \times 10^3, 4.96 \times 10^3$ rad./sec.
$= 2.68$ KHz., 789 Hz.

$\frac{D^2R}{(2D - 1)L} = 8.25 \times 10^3$ rad./sec.
$= 1.31$ kHz = voltage loop zero

$\frac{2(1 - D)}{RC} = 12 \times 10^3$ rad./sec.
$= 1.91$ kHz. = current loop zero

Case 2:

for $R = 1025\Omega$, $\frac{L}{RD^2} = .052 \times 10^{-3}$ (assuming that D remains almost unchanged for continuous current)

The poles are now complex, but the resonant frequency is still

$\omega n = \frac{D}{\sqrt{LC}} = 9.2 \times 10^3$ rad./sec.

$fn = 1.46$ kHz

$\frac{D^2R}{(2D - 1)L} = 41.25 \times 10^3$ rad./sec.
$= 6.57$ kHz. = voltage loop zero

$\frac{2(1 - D)}{RC} = 2.4 \times 10^3$ rad./sec.
$= 380$ Hz. = current loop zero

For the voltage loop, Case 1 indicates that the zero is helpful at full load because it compensates for the phase shift of one of the poles. However, at 20% load the zero frequency is so high that it is of little use, and the regulator may be

unstable at light loads unless it is lag compensated so that the gain is much less than 1.0 at 1.46 kHz. This was observed experimentally when $K_{1(s)}$ originally had a transfer function of the form,

$$K_{1(s)} = A_1 \frac{\left(1 + \frac{s}{s_1}\right)}{s}$$

With the above $K_{1(s)}$, the circuit was stable at full load because the zero kept the net phase shift below 180° at the unity gain frequency. However, at light loads, the zero was at such a high frequency that it provided no significant compensation, and the converter was unstable. Stability over the full load range was achieved by changing $K_{1(s)}$ to a lag compensator of the form,

$$K_{1(s)} = \frac{A_1}{s}$$

This attenuated the gain to well below 1.0 at the natural resonance frequency.

Equation (II-59) and the two above cases indicate that the current loop should be easier to compensate since the zero of the uncompensated loop decreases with the load, and the dc open loop gain also decreases with load.

III. STABILITY ANALYSIS OF TWO BUCK CONVERTERS IN PARALLEL

In high power applications it is often convenient to modularize a DC power supply by connecting several identical converter modules in parallel. Modularized designs also possess a reliability advantage in that faulted modules may be removed so that operation may continue at a somewhat reduced power level. These systems operate in the conventional manner where one module provides voltage regulation, and the others will either be cut-off or operate in their current limit mode. It is also good practice to synchronize the switching frequency for each module to reduce EMI induced errors in the controllers.

To analyze the stability of these systems, it is often assumed that it is adequate to simply measure the open loop gain and phase of the individual modules. The assumption is that if the individual modules are stable, the system will be stable when the modules are connected in parallel. This usually seems to work in practice, but there appears to be no analytical basis for this assumption. This conclusion can be illustrated by the linearized state space model for two buck converters in parallel. Buck converters were chosen for this analysis because,

1. Their small signal open loop gain is identical to a PPCF converter with the secondary of its inductor connected to the output.
2. The small signal open loop gain of the buck is adequate to show the problems involved, and it is less complex than the PPCF with the inductor secondary connected to the input.

Voltage Regulation Loop

Fig. III-1 shows the simplified schematic for a buck converter, which is assumed to be in the voltage regulation mode. Various references such as Mitchell [14.] have presented the small signal open loop gain function, which can be derived using state space averaging and linearization,

$$G_{(s)}H_{(s)V} = \frac{\frac{V_1 K_{1(s)} H_1}{V_P}}{LCs^2 + \frac{Ls}{R} + 1} \qquad \text{(III-1)}$$

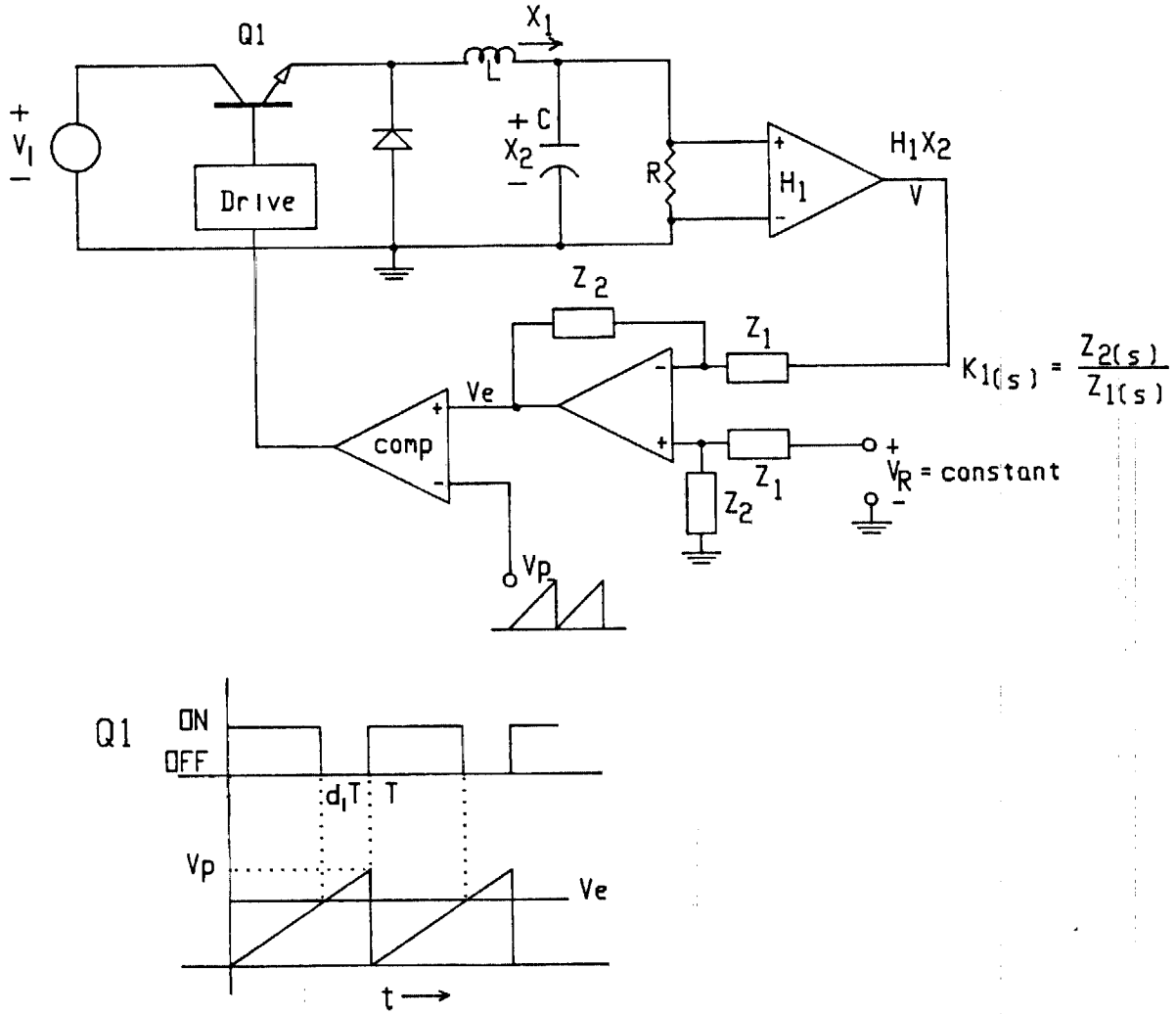


Fig.Ⅲ-1. PWM control for buck converter in voltage regulation mode.

Fig. III-2 shows a small signal equivalent circuit for the open loop transfer function given by (III-1). Note that this model includes a voltage source that is dependent on $x_{2(s)}$.

Current Regulation Loop

The simplified schematic for a buck converter in the current regulation model is shown in Fig. III-3. The differential equations for the two conduction intervals are,

Interval #1: $0 \le t \le d_2T$

$$\dot{x}_1 = -\frac{x_2}{L} + \frac{V_1}{L} \qquad \text{(III-2)}$$

$$\dot{x}_2 = \frac{x_1}{C} - \frac{x_2}{RC} \qquad \text{(III-3)}$$

$$\text{or} \quad \dot{\underline{x}} = A_1 \underline{x} + B_1 V_1 \qquad \text{(III-4)}$$

$$\text{where} \quad A_1 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \qquad \text{(III-5)}$$

$$B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \qquad \text{(III-6)}$$

Interval #2: $d_2T \le t \le T$

$$\dot{x}_1 = \frac{-x_2}{L} \qquad \text{(III-7)}$$

$$\dot{x}_2 = \frac{x_1}{C} - \frac{x_2}{RC} \qquad \text{(III-8)}$$

$$\text{or} \quad \dot{\underline{x}} = A_2 \underline{x} + B_2 V_1 \qquad \text{(III-9)}$$

$$\text{where} \quad A_2 = A_1 \qquad \text{(III-10)}$$

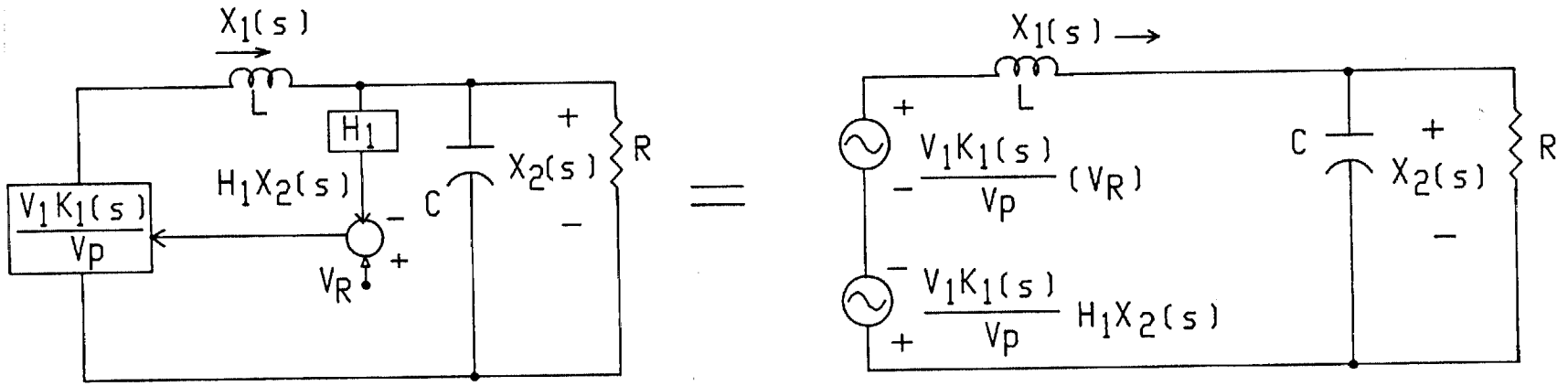


Fig. III-2. Small signal model for the buck converter in voltage regulation mode.

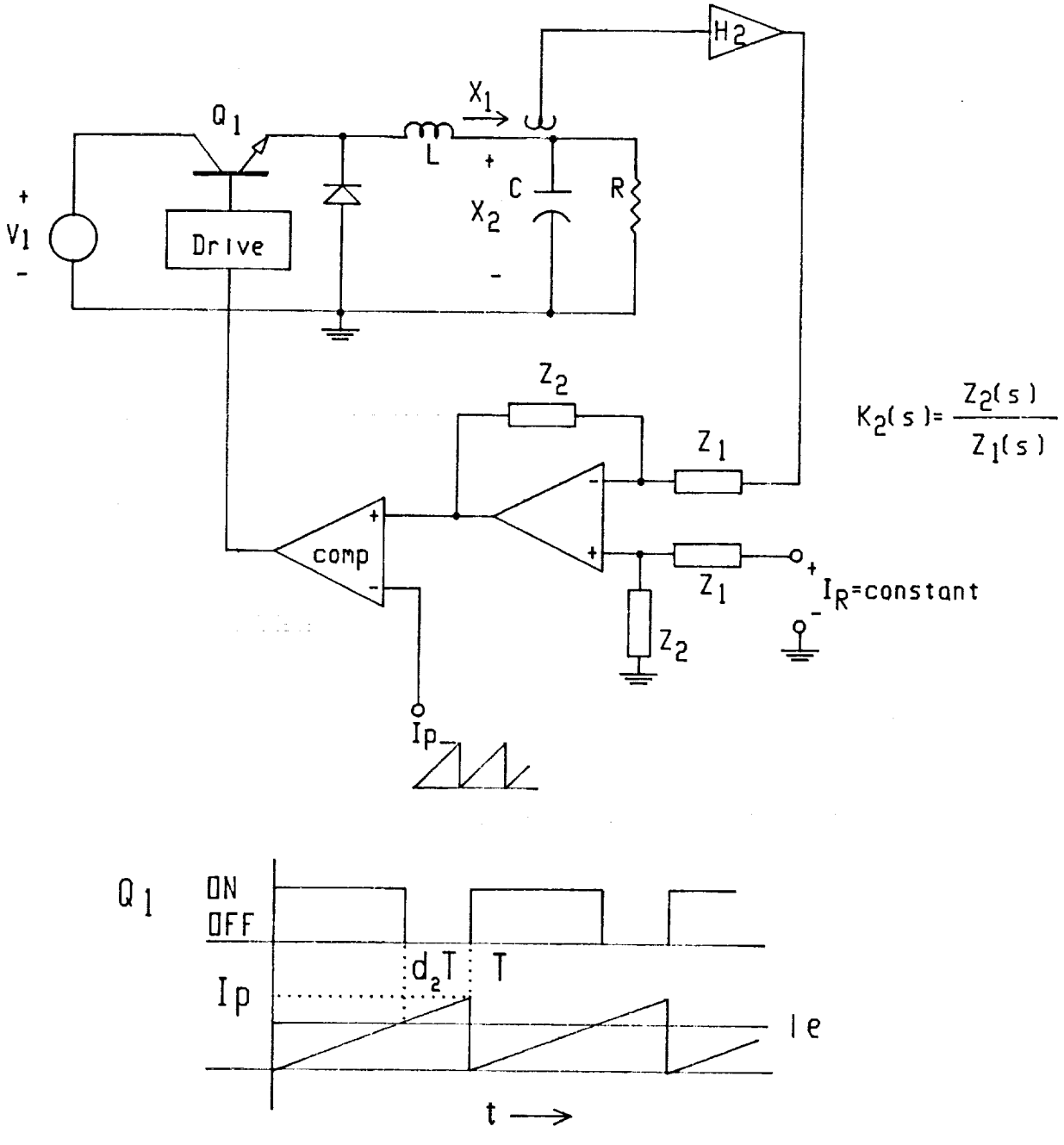


Fig.Ⅲ-3. PWM control for buck converter in the current regulation mode.

$$B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \qquad \text{(III-11)}$$

We can write the following approximate derivatives if the switching frequency is high with respect to the natural frequencies of the circuit and any signal frequencies,

$$\dot{\underline{x}}(0) = \frac{\underline{x}(d_2T) - \underline{x}(0)}{d_2T} \qquad \text{(III-12)}$$

$$\dot{\underline{x}}(d_2T) = \frac{\underline{x}(T) - x(d_2T)}{1 - d_2T} \qquad \text{(III-13)}$$

From the previous equations we have,

$$\underline{x}(d_2T) = \underline{x}(0) + d_2T\left(A_1\,\underline{x}(0) + B_1\,V_1\right) \qquad \text{(III-14)}$$

$$\underline{x}(T) = \underline{x}(d_2T) + T(1 - d_2)\left(A_2\,\underline{x}(d_2T) + B_2\,V_1\right) \qquad \text{(III-15)}$$

Substituting (III-14) into (III-15),

$$\underline{x}(T) = \left[\underline{x}(0)(1 + d_2\,T\,A_1) + d_2\,T\,B_1\,V_1\right]\left[1 + T(1 - d_2)\,A_2\right] + T(1 - d_2)\,B_2\,V_1 \qquad \text{(III-16)}$$

Re-arranging (III-16),

$$\frac{\underline{x}(T) - \underline{x}(0)}{T} = \underline{x}(0)\left[(1 - d_2)\,A_2 + d_2\,A_1 + d_2\,A_1\,(1 - d_2)\,A_2\,T\right] + V_1\left[d_2\,B_1 + d_2\,B_1\,(1 - d_2)\,A_2\,T + (1 - d_2)\,B_2\right] \qquad \text{(III-17)}$$

Assuming that a high switching frequency is equivalent to taking the limit (III-17) as $T \rightarrow 0$,

$$\lim_{T \rightarrow 0}\left(\frac{\underline{x}(T) - \underline{x}(0)}{T}\right) = \dot{\underline{x}} = \left[d_2\,A_1 + (1 - d_2)\,A_2\right]\underline{x} + \left[d_2\,B_1 + (1 - d_2)\,B_2\right]V_1 \qquad \text{(III-18)}$$

(III-18) can then be written,

$$\dot{\underline{x}} = A_1\,\underline{x} + B_1\,d_2\,V_1 \qquad \text{(III-19)}$$

We now assume that $\underline{x}$ and d_2 can be divided into constant ($\underline{x}_0$, D_2) and time varying ($\hat{\underline{x}}$, $\hat{d}_2$) components,

$$\underline{x} = \underline{x}_0 + \hat{\underline{x}} \ , \ d_2 = D_2 + \hat{d}_2 \qquad \text{(III-20)}$$

(III-19) becomes,

$$\dot{\hat{\underline{x}}} = A_1 (\underline{x}_0 + \hat{\underline{x}}) + B_1 (D_2 + \hat{d}_2) V_1 \qquad \text{(III-21)}$$

D. C. component: $\underline{0} = A_1 \underline{x}_0 + B_0 V_1$ (III-22)

where $B_0 \equiv B_1 D_2$ (III-23)

A. C. component: $\dot{\hat{\underline{x}}} = A_1 \hat{\underline{x}} + E \hat{d}_2$ (III-24)

where $E \equiv V_1 B_1 = \begin{bmatrix} \frac{V_1}{L} \\ 0 \end{bmatrix}$ (III-25)

Taking the Laplace transform of (III-24)

$$\hat{\underline{x}}_{(s)} = (sI - A_1)^{-1} E \hat{d}_{2(s)} \qquad \text{(III-26)}$$

We know that $\hat{d}_{2(s)}$ will depend on $\hat{x}_{1(s)}$ because of the current feedback loop. After linearization we can express the general control law in the following form,

$$\hat{d}_{2(s)} = F^T_{(s)} \hat{\underline{x}}_{(s)} \qquad \text{(III-27)}$$

From Fig. (III-3) we have,

$$d_2 = \frac{i_c}{I_P} \qquad \text{(III-28)}$$

Taking the Laplace transform,

$$d_{2(s)} = \frac{I_{c(s)}}{I_P} = \frac{K_{2(s)} V_R - K_{2(s)} H_2 X_{1(s)}}{I_P} \qquad \text{(III-29)}$$

Therefore, for the time varying part, $\hat{d}_2$,

$$\hat{d}_{2(s)} = - \frac{K_{2(s)} H_2 \hat{x}_{1(s)}}{I_P} \qquad \text{(III-30)}$$

From (III-27) and (III-30),

$$F^T_{(s)} = \left[\frac{-K_{2(s)} H_2}{I_P} \quad 0\right] \tag{III-31}$$

We now wish to open the control loop mathematically by replacing $\hat{\underline{x}}_{(s)}$ in (III-27) with an independent vector $\hat{\underline{V}}_{(s)}$. Thus,

$$\hat{d}_{2(s)} = F^T_{(s)} \hat{\underline{V}}_{(s)} \tag{III-32}$$

and from (III-26 and 32),

$$\hat{\underline{x}}_{(s)} = (sI - A_1)^{-1} E F^T_{(s)} \hat{\underline{V}}_{(s)} \tag{III-33}$$

Therefore, the general ac open-loop transfer function matrix, $T_{xv\,(s)}$, is,

$$T_{xv\,(s)} \equiv (sI - A_1)^{-1} E F^T_{(s)} \tag{III-34}$$

From (III-25) and III-31),

$$E F^T_{(s)} = \begin{bmatrix} \frac{-K_{2(s)} H_2 V_1}{I_P L} & 0 \\ 0 & 0 \end{bmatrix} \tag{III-35}$$

Now,

$$(sI - A_1)^{-1} = \frac{\begin{bmatrix} \left(s + \frac{1}{RC}\right) & -\frac{1}{L} \\ \frac{1}{C} & s \end{bmatrix}}{s^2 + \frac{s}{RC} + \frac{1}{LC}} \tag{III-36}$$

$$(sI - A_1)^{-1} E F^T_{(s)} = \frac{\begin{bmatrix} -\frac{K_{2(s)} H_2 V_1}{I_P L}\left(s + \frac{1}{RC}\right) & 0 \\ \frac{-K_{2(s)} H_2 V_1}{I_P LC} & 0 \end{bmatrix}}{s^2 + \frac{s}{RC} + \frac{1}{LC}} \tag{III-37}$$

From (III-37) the small signal open loop current gain transfer function is,

$$G_{(s)} H_{(s)I} = \frac{\frac{K_{2(s)} H_2 V_1}{I_P R}(sRC + 1)}{s^2 LC + \frac{sL}{R} + 1} \tag{III-38}$$

Equation (III-38) can be used to derive the small signal equivalent circuit shown in Fig. III-4. Note that this model includes a voltage source that is dependent on $x_{1(s)}$.

Parallel Operation

If the outputs of the two circuits in Figs. III-2 and 4 are connected in parallel, the circuit in Fig. III-5 results. Note that the current from the voltage regulated converter is now designated x'_1 to distinguish it from the current of the current regulated converter. It is seen that the system complexity has increased considerably because the two circuits now load each other, and superposition cannot be applied directly to the two dependent voltage sources. However, it is possible to simplify the system somewhat by deriving equivalent circuits for that portion to the left of a a' and to the right of b b'. The simplified equivalent circuits and definitions of terms are shown in Fig. III-6. From Fig. III-6(a.),

$$-x'_1 = (x_2 + A_1 x_2 - V_{RI})\, y_1 = (x_2 - V_{R1})y_1 + x_2 (A_1 y_1) \qquad \text{(III-39)}$$

which yields the equivalent circuit in Fig. III-7 (a.). From Fig. III-6 (b),

$$-x_1 = (x_2 + A_2 x_1 - V_{R2})\, y_1 \qquad \text{(III-40)}$$

$$-x_1 (1 + A_2 y_1) = x_2 y_1 - V_{R2} y_1 \qquad \text{(III-41)}$$

$$-x_1 = x_2 \left(\frac{y_1}{1 + A_2 y_1}\right) - V_{R2} \left(\frac{y_1}{1 + A_2 y_1}\right) \qquad \text{(III-42)}$$

which yields the equivalent circuit in Fig. III-7 (b.).

The equivalent circuits from Fig. III-7 can now be used in Fig. III-5 to produce the result in Fig. III-8. The closed loop transfer function for the equivalent system in Fig. III-8 can be derived by writing a single nodal equation using x_2,

$$x_2 \left(y_1 + A_1 y_1 + y_2 + \frac{y_1}{1 + A_2 y_1}\right) = V_{R1} y_1 + \frac{V_{R2} y_1}{1 + A_2 y_1} \qquad \text{(III-43)}$$

$$x_2 = \frac{V_{R1} y_1 (1 + A_2 y_1) + V_{R2} y_1}{2y_1 + A_1 y_1 + y_2 + A_2 y_1^2 + A_1 A_2 y_1^2 + A_2 y_1 y_2} \qquad \text{(III-44)}$$

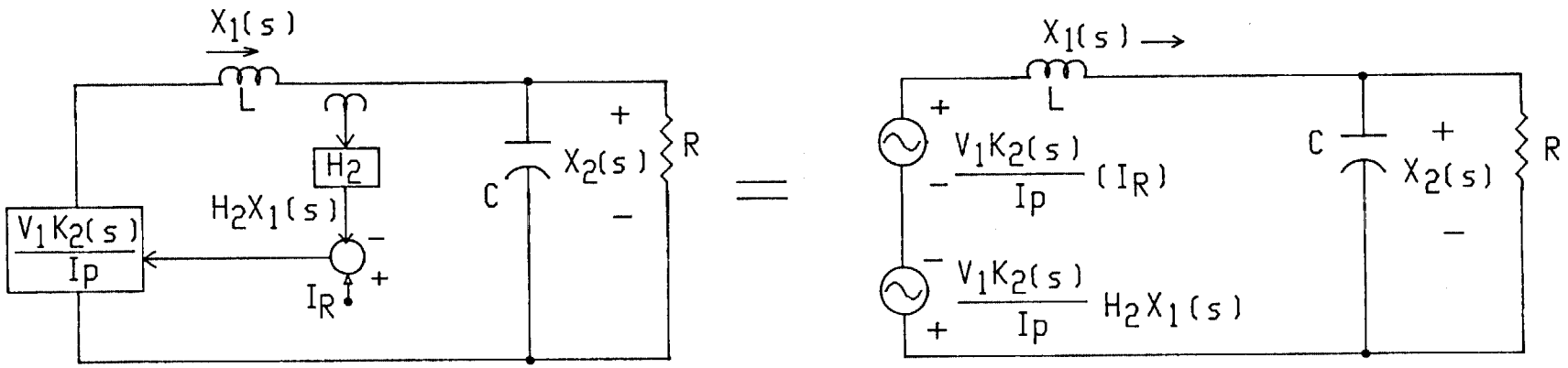


FIG.Ⅲ-4. Small signal model for the buck converter in current regulation mode.

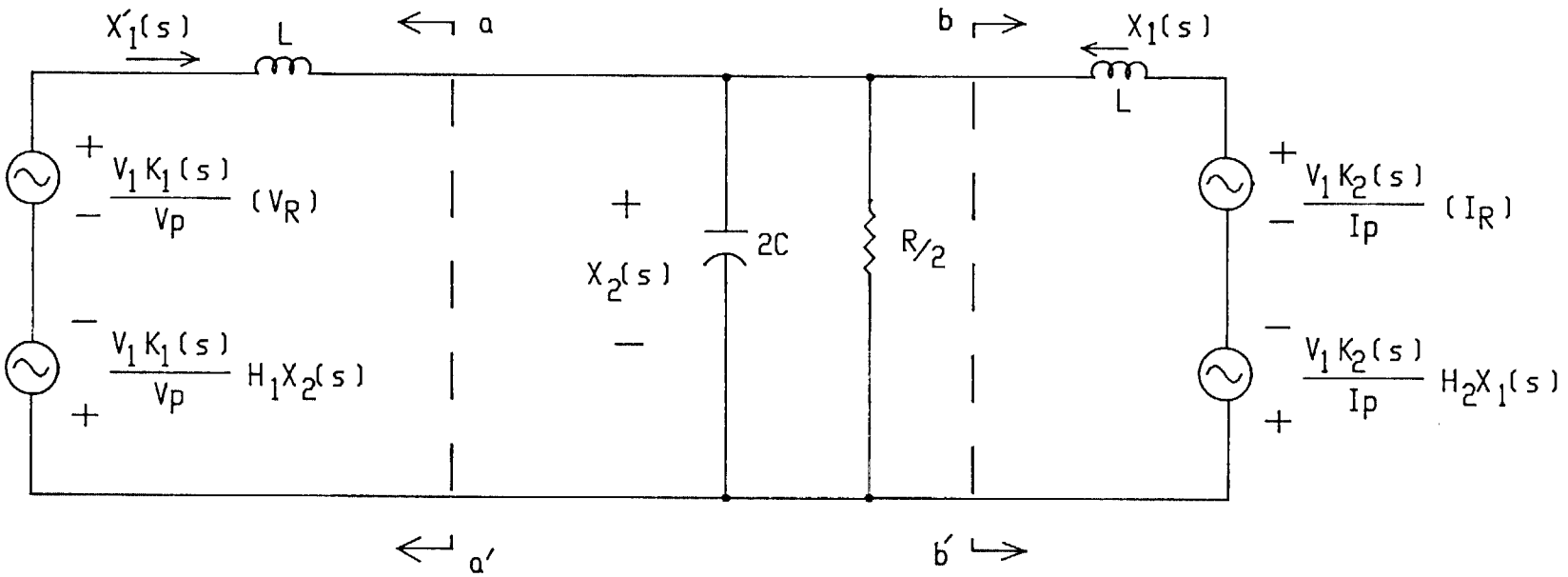
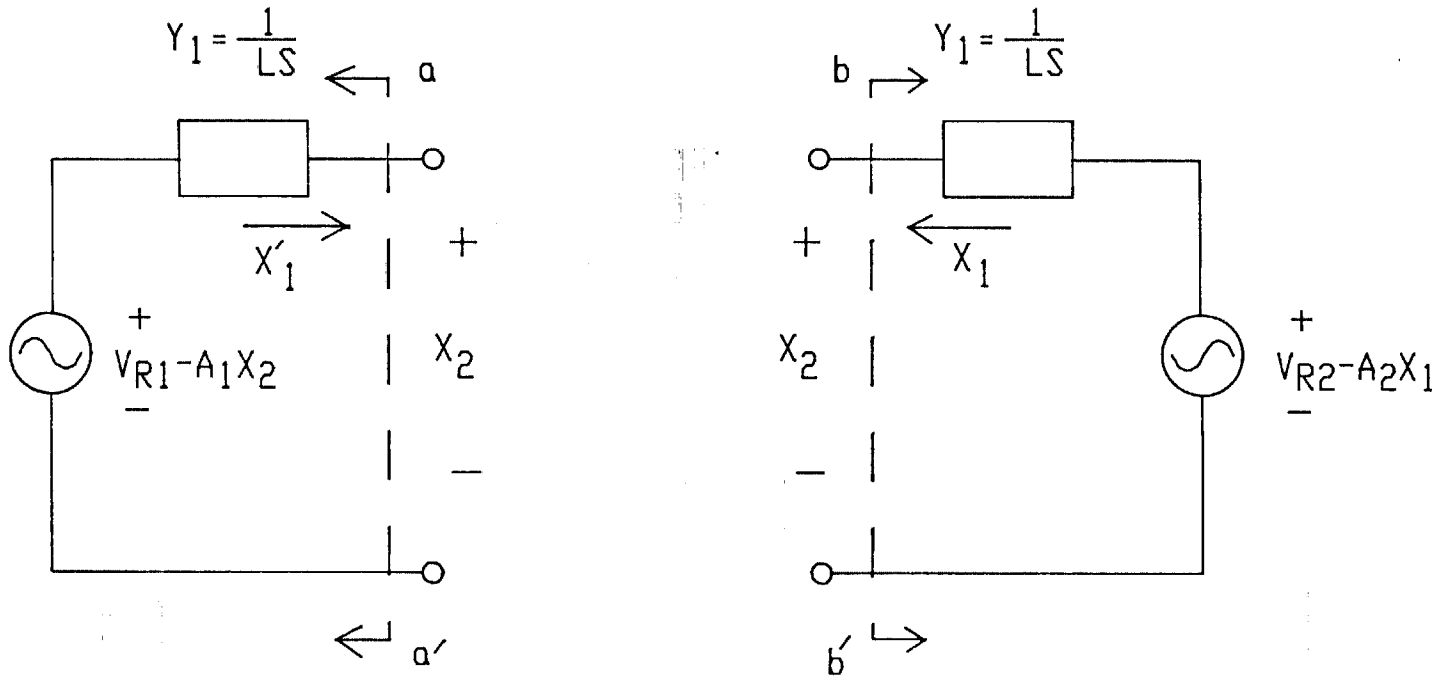


FIG.Ⅲ-5. Small signal model for two parallel buck converters, one in the voltage regulation mode and one in the current regulation mode.



$$V_{R1} \equiv \frac{V_1 K_1(s)}{V_p} V_R$$

$$A_1 \equiv \frac{V_1 K_1(s)}{V_p} H_1$$

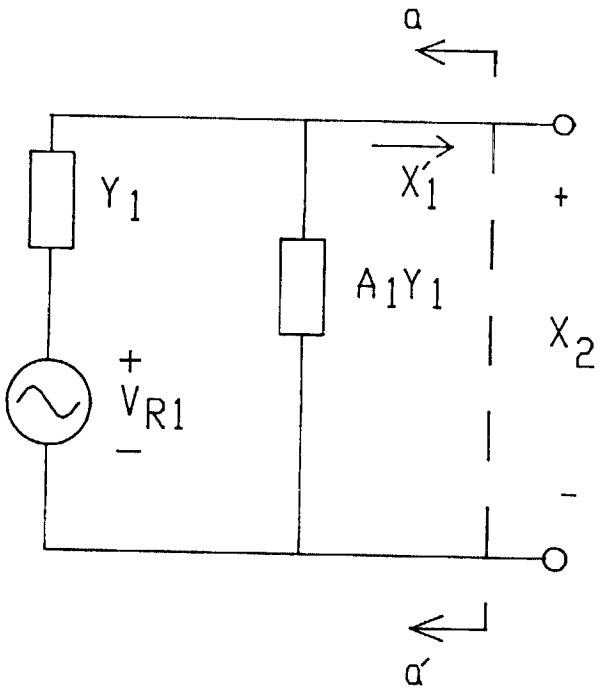
(a.) Left of aa′

$$V_{R2} \equiv \frac{V_1 K_2(s)}{I_p} I_R$$

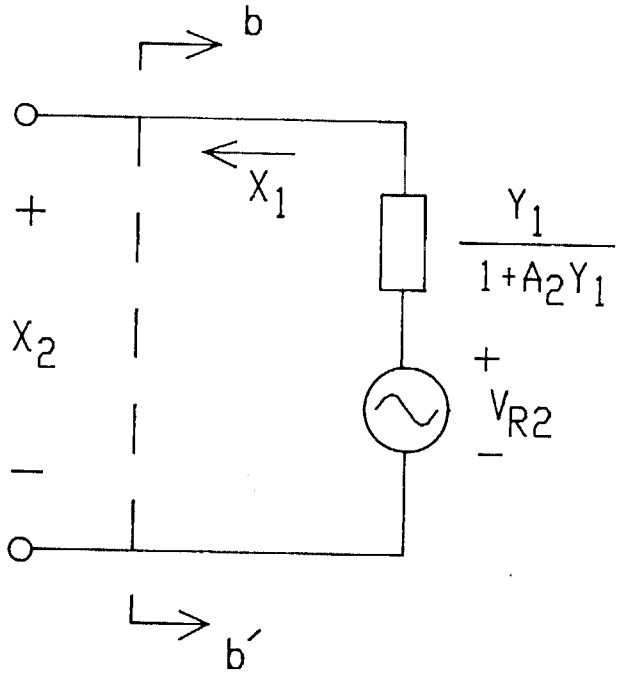
$$A_2 \equiv \frac{V_1 K_2(s)}{I_p} H_2$$

(b.) Right of bb′

FIG.Ⅲ-6. Simplified equivalent circuits from FIG.Ⅲ-5.



(a.) Left of aa'



(b.) Right of bb'

FIG. Ⅲ-7. Equivalent circuits to eliminate dependent voltage sources.

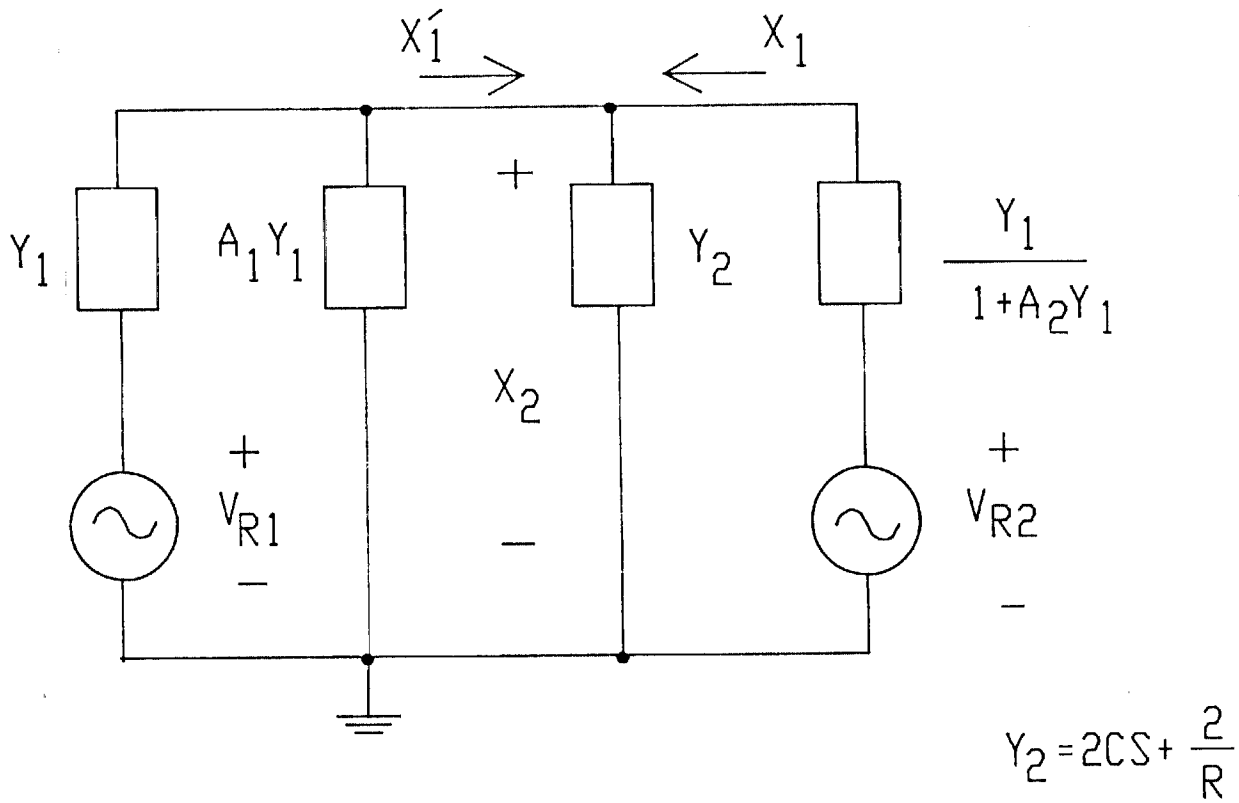


FIG. III-8. Equivalent circuit for complete system without dependent voltage sources.

The characteristic equation of the system is obtained by setting the denominator of (III-44) equal to zero,

$$2y_1 + A_1 y_1 + y_2 + A_2 y_1^2 + A_1 A_2 y_1^2 + A_2 y_1 y_2 = 0 \qquad \text{(III-45)}$$

Thus we know that the system will be stable if and only if none of the roots of (III-45) are in the right half s-plane or on the imaginary axis. This can be determined by using Routh's criterion or by using a computer program to calculate the roots. However, these methods are strictly analytical, and they do not provide information about the relative stability such as the gain and phase margins that can be verified experimentally from a Bode plot. If the voltage loop is opened and excited by V_{T1} while the current loop is closed we obtain,

$$\frac{x_2}{V_{T1}} = \frac{-A_1 y_1 - A_1 A_2 y_1^2}{2y_1 + y_2 + A_2 y_1^2 + A_2 y_1 y_2} \qquad \text{(III-46)}$$

And if the current loop is opened and excited by V_{T2} while the voltage loop is closed,

$$\frac{x_2}{V_{T2}} = \frac{-A_2 y_1}{2 y_1 + A_1 y_1 + y_2} \qquad \text{(III-47)}$$

If the L.H.S. of (III-45) could be obtained from some combination of the R.H.S.'s of (III-46) and (III-47), relative stability could be determined experimentally, but there is no readily apparent way to do this.

Thus it appears that the stability analysis will depend on the calculated values of the roots of (III-45) instead of phase and gain measurements. Time constraints did not permit further study of this problem, but it should be recognized that additional work is needed to provide more accurate methods for determining the stability of parallel converter systems.

IV. EXPERIMENTAL RESULTS FOR THE PUSH-PULL CURRENT-FED CONVERTER

2700 Watt Push-Pull Current-Fed Converter Circuit Description

1. System Block Diagram. The block diagram of a 2700 watt converter system is shown in Fig. IV-1, and individual schematics are shown in Figs. IV-3-9. This system is composed of three 900 watt converter modules operating in parallel in the conventional manner with current limit controllers. Since there will always be a slight difference in the calibrated output voltages, assume that $V_{01} > V_{02} > V_{03}$. Therefore a light loads only Mod #1 is active, and it regulates the output voltage at V_{01}. As the load increases, Mod #1 goes into current limit at I_{01}, and Mod #2 regulates the output voltage at V_{02}. This continues for further load increases, as indicated in Fig. IV-2. Eventually all three modules will be in current limit.

2. Converter Module. The schematic for each of the three converter modules is shown in Fig. IV-3. This circuit is a push-pull current-fed converter with the secondary of the energy storage reactor, L1, feeding the input [2-4]. This topology was chosen for the following reasons:

   a.) As discussed earlier, a forced commutation circuit was chosen to eliminate the rather large series capacitor that is present with series resonant designs. High frequency foil type capacitors such as polypropolene have serious temperature limitations and also may be quite vulnerable to the radiation within the vicinity of a nuclear reactor. Naturally, other components also will be vulnerable to such an environment, but it was decided that these capacitors should not be the limiting component. Bipolar transistors were chosen over other types of switches since their T_J max is commonly rated at 200°C instead of the 125°C or 150°C ratings of other devices.

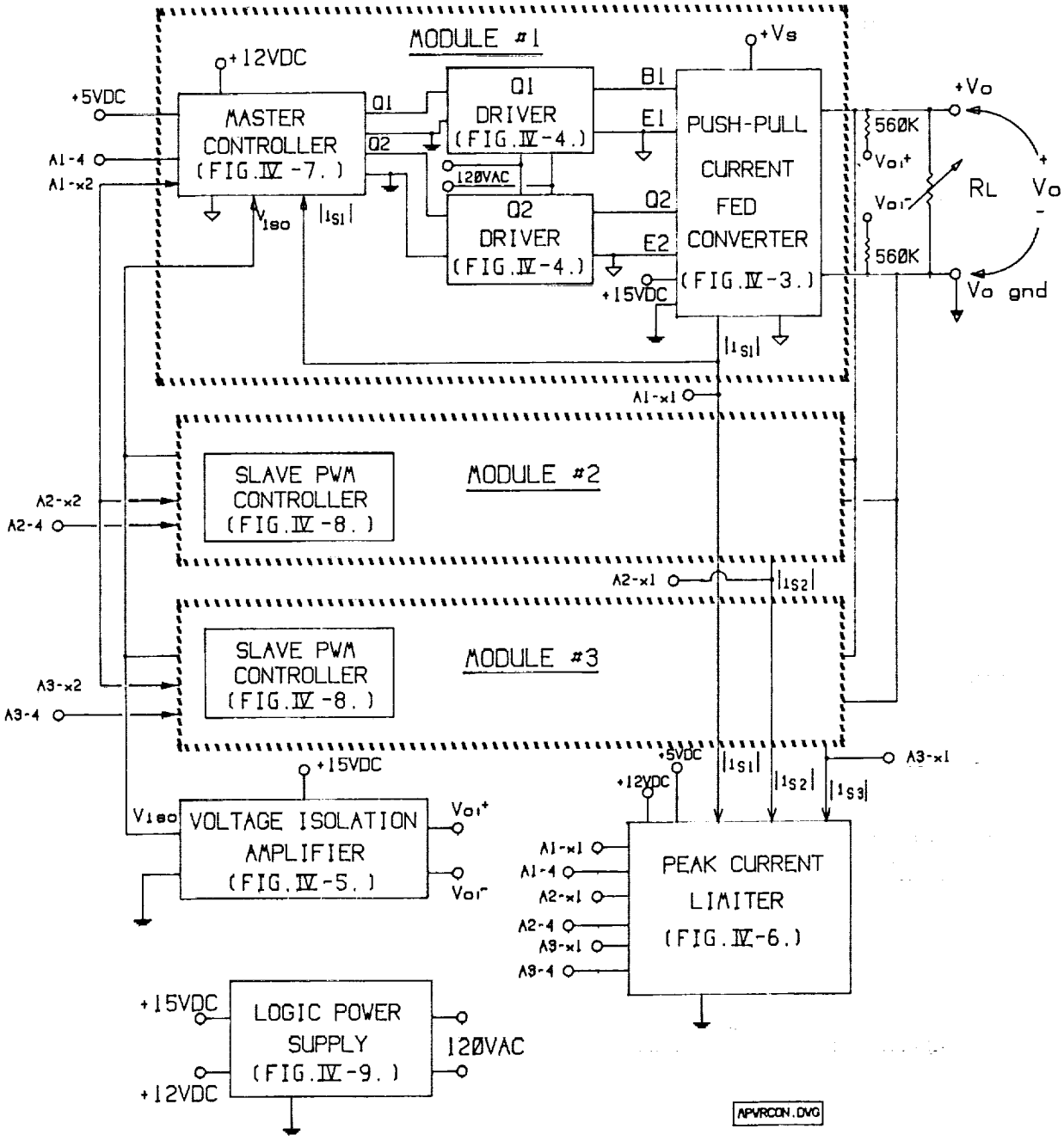


FIG.Ⅳ-1. MODULARIZED POWER CONVERTER

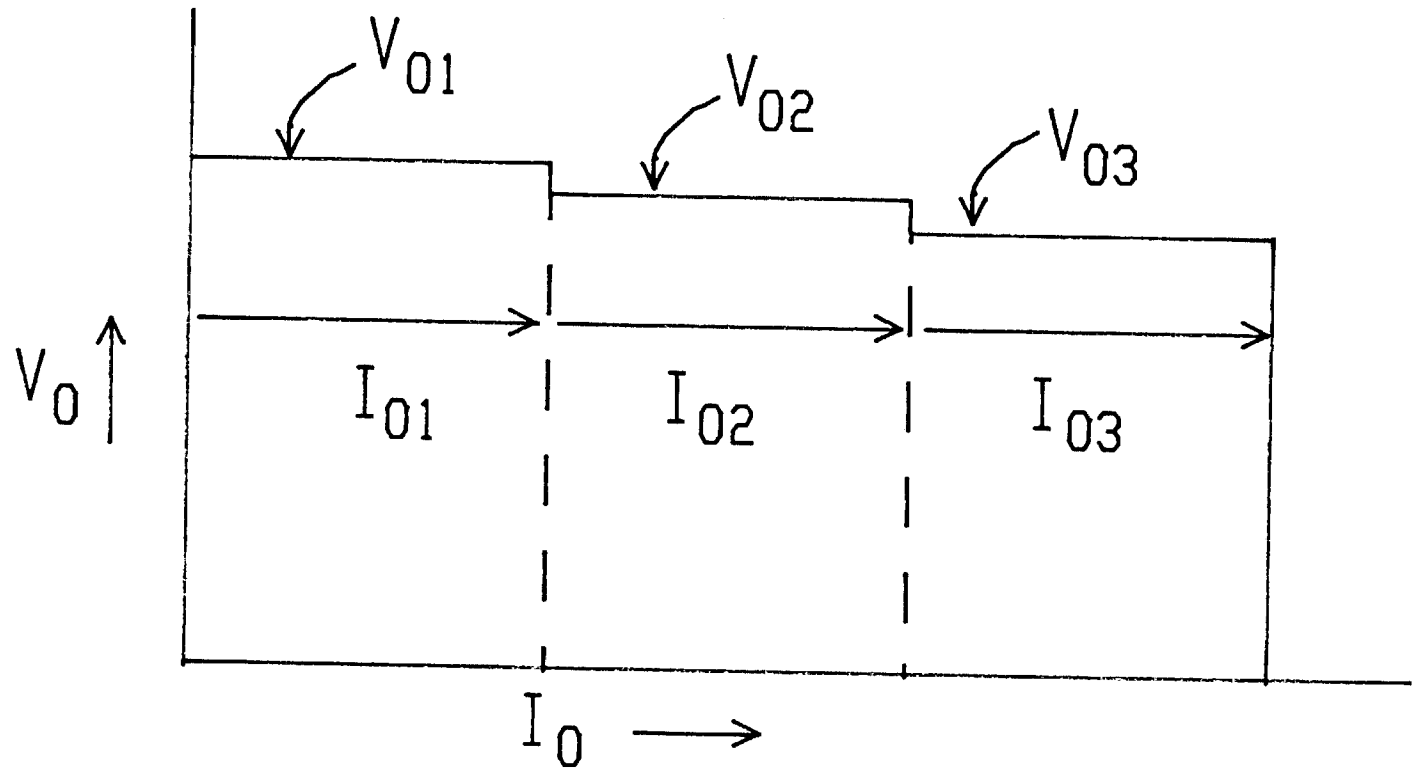
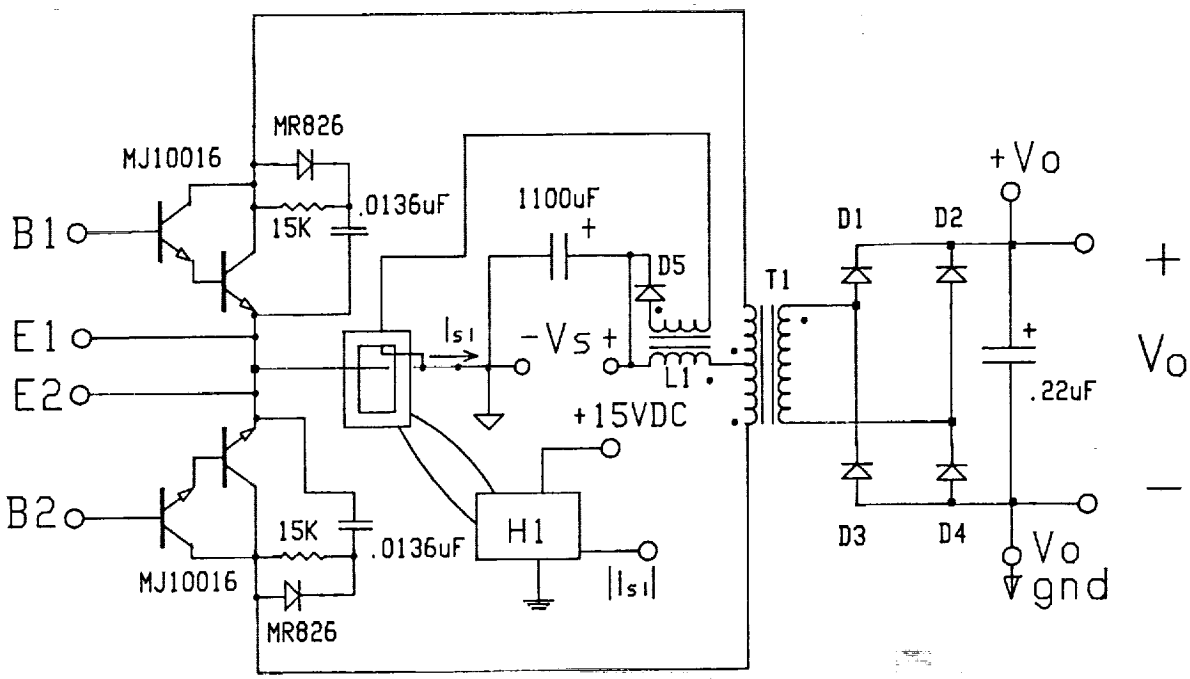


FIG.Ⅳ-2. Vo vs. Io for 3 parallel converters.



Vs=115Vdc, Vo=410Vdc
T1:n=1:4.87, bifilar
L1:1.22mH, n=1.1, bifilar
D1-D4:MR1376
D5:MR1386
H1:LEM-LA 50-P Hall effect sensor

FIG.Ⅳ-3. PUSH-PULL CURRENT FED CONVERTER MODULE

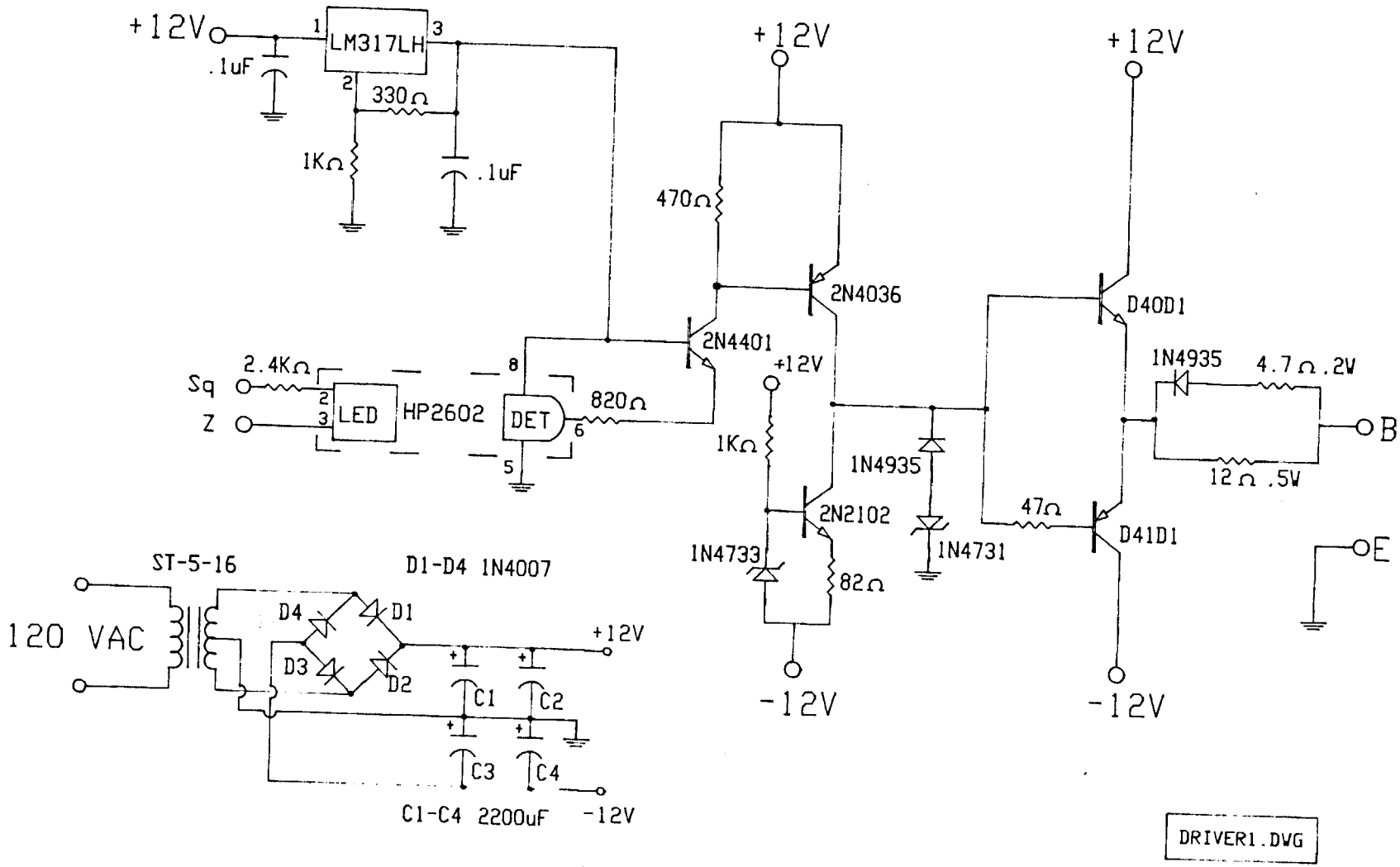
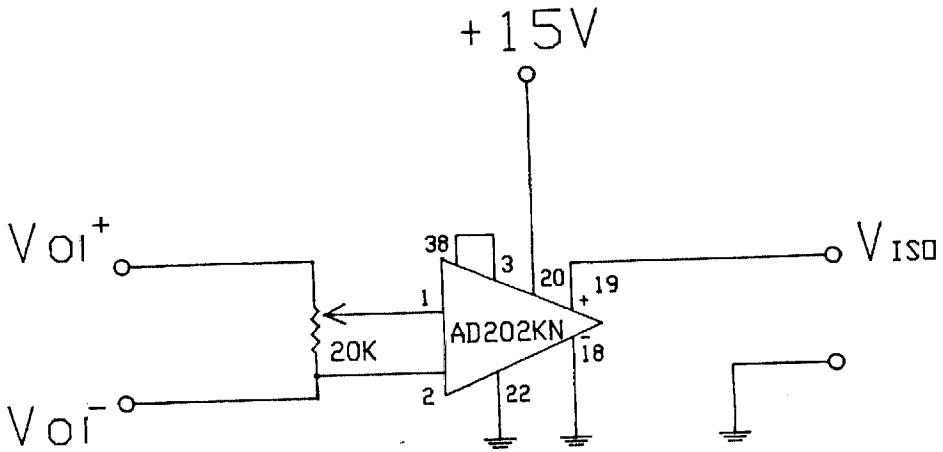


FIG. Ⅳ-4. BIPOLAR DRIVE CIRCUIT



VISOAMP.DWG

FIG.Ⅳ-5. VOLTAGE ISOLATION AMPLIFIER

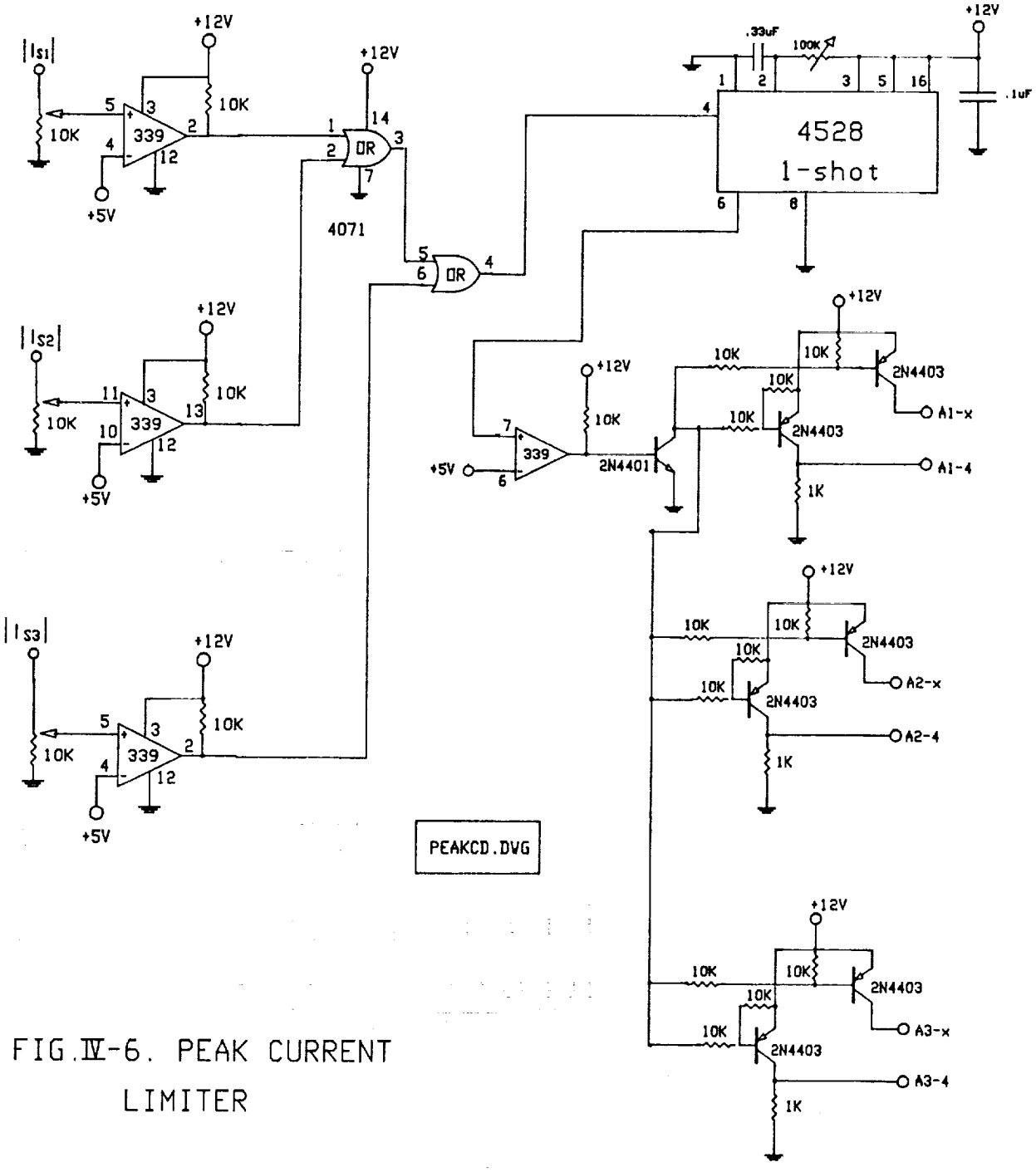


FIG.Ⅳ-6. PEAK CURRENT LIMITER

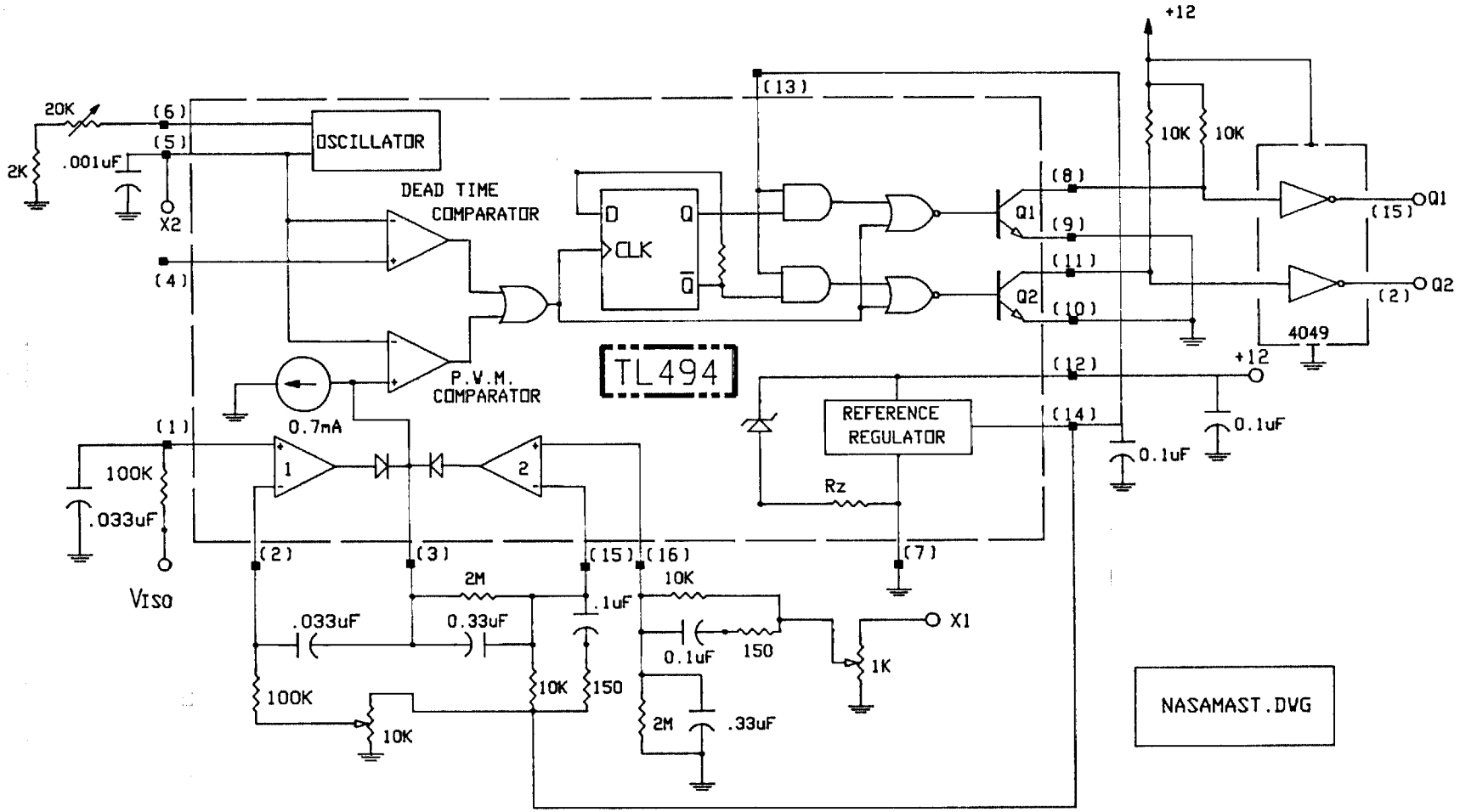


FIG. Ⅳ-7. MASTER PWM CONTROLLER, A1

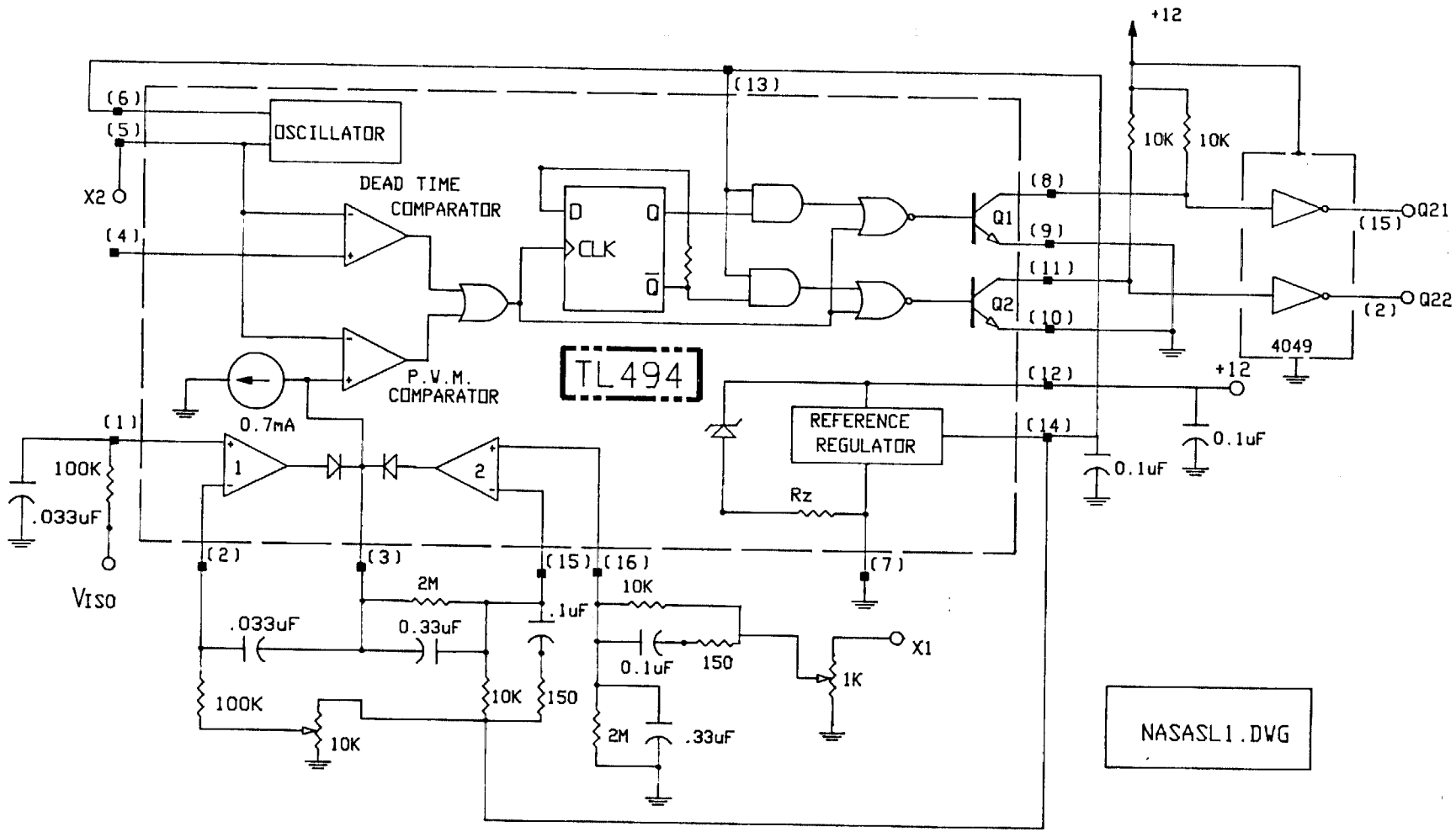


FIG. Ⅳ-8. SLAVE PWM CONTROLLER, A2 AND A3

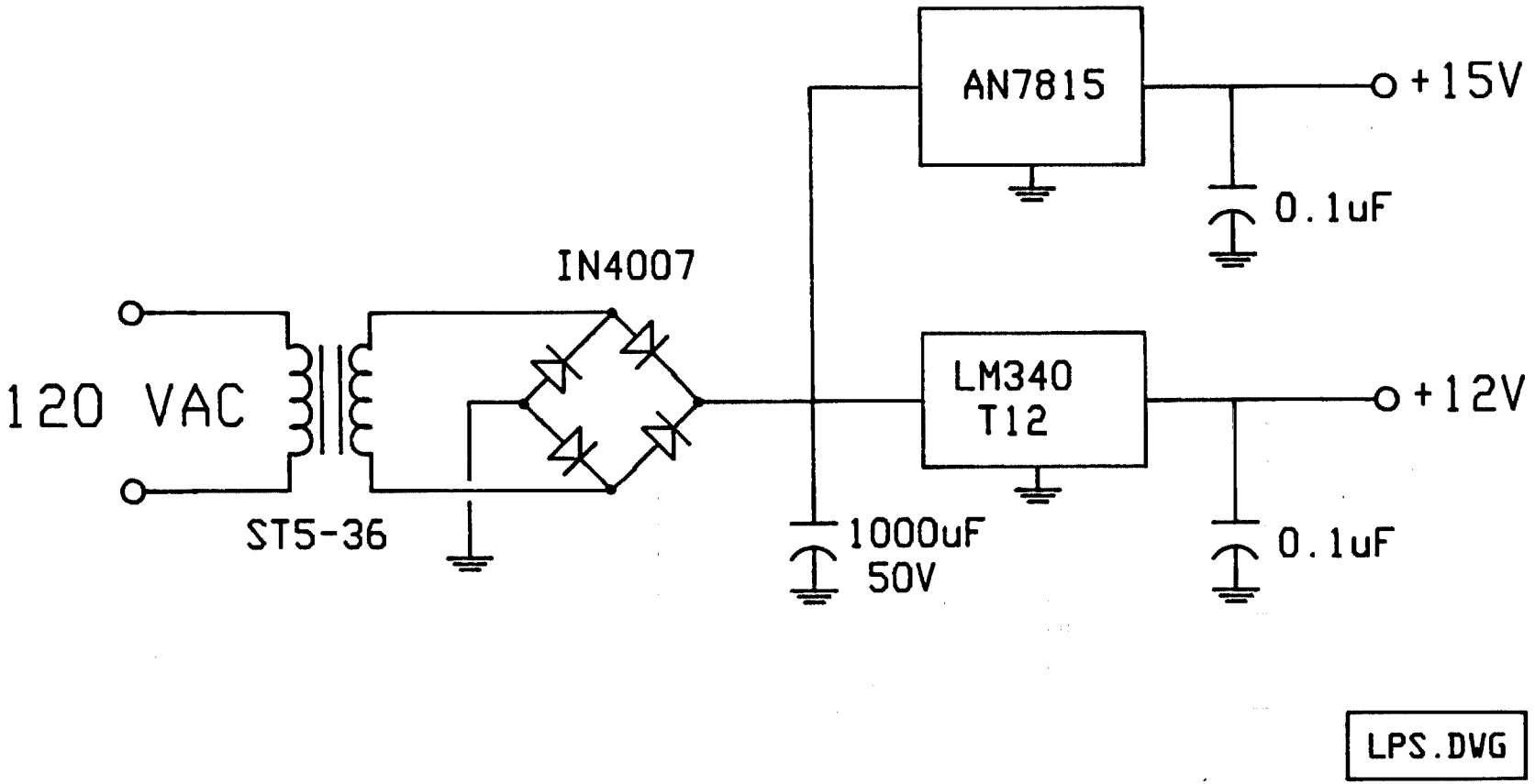


FIG. Ⅳ-9. LOGIC POWER SUPPLY

b.) L1 provides a means of eliminating current transients due to transformer saturation caused by a flux imbalance or simultaneous conduction of Q1 and Q2. This allows the use of voltage mode control instead of the somewhat more complex current mode control which would be necessary with other topologies. As pointed out in [2-4], it is also possible to connect the secondary of L1 to the output instead of the input. Normally, this would be the preferred connection since the stored energy in L1 is transferred to the load instead of being circulated back to the input. Since all energy flows to the load, it is likely that this alternate connection would be slightly more efficient. However, for the output connection L1 needs a turns ratio that is about the same as T1, which is 1:4.87. This means that D1 will experience reverse voltages in the 1000 volt range. The output connection was attempted but was discarded because of the difficulty in finding high speed switching diode for D5 that had an adequate voltage rating. Diodes such as the Powerex R502 series are available with t_{rr}=1.5 μs. and V_{RRM}=1200 V., but their 80 amp rating is much larger than required, and they are much slower than the MR1386 with a t_{rr}=0.2μs. which was ultimately used.

c.) With the proper controller, this circuit can be operated in the buck or boost modes. This feature might be useful since a short circuit failure in a thermoelectric module can reduce V_s to 0.5 V_s. If the converter is specified to operate in the buck mode at the full value of V_s, it can deliver half power in the boost mode for an emergency input of 0.5 V_s. This is achieved without imposing any extreme specification penalties on the components. This initial project was primarily concerned with operation at full input, so only the buck controller was built and tested. However, the option of buck-boost control could be implemented if the need for it is deemed necessary. It should be mentioned that switching losses for this topology are somewhat higher than those for a full bridge converter. In a full bridge, energy trapped in the transformer primary leakage inductance is circulated back to the input capacitor by means

diodes in anti-parallel with the transistors. In the present circuit, there is no way to recover the energy stored in the primary leakage inductance of T1 and L1, so it must be dissipated by the snubbers. At 10 kHz, the unoptimized efficiency of this circuit was 91.1%. Another disadvantage to this circuit is the relatively high $v_{CE(max)}$ that appears across the transistors. Even with no turn-off transient, this voltage is about 3 V_{IN} because of the voltage coupling of T1 and L1. The turn-off transient will make $v_{CE(max)}$ even higher of course, especially because of the trapped energy in the leakage inductance of L1 and T1. In comparison, $v_{CE(max)}$ for a full bridge is only V_{IN} plus the turn-off transient. For V_{IN}=115 Vdc at full load $v_{CE(max)}$ for this circuit was about 400 volts peak. Power transistors are readily available in this voltage range, but the selection will be much more limited for higher input voltages.

3. Bipolar Drive Circuit. The schematic for each of the six transistor drive circuits is shown in Fig. IV-4. This circuit provides optical coupling to isolate the control logic from the power circuit. This helps to prevent EMI from the power circuit from interfering with the control logic. A negative bias is also employed to minimize the turn-off time of the bipolars.

4. Voltage Isolation Amplifier. This amplifier is shown in Fig. IV-5. Its purpose is to isolate the power output from the control logic to help prevent EMI from interfering with the controller.

5. Peak Current Limiter. This circuit is shown in Fig. IV-6. As explained earlier, average current limiting is employed for thermal protection and to allow parallel operation of several converter modules. However, it is doubtful that this circuit is fast enough to provide protection from the high instantaneous load currents that result from an abrupt short circuit. Therefore, the instantaneous current limit circuit in Fig. IV-6 is used to provide rapid protection from an abrupt fault. If the instantaneous value of $|I_{s1}|$, $|I_{s2}|$, or $|I_{s3}|$ reaches a specified value, the one-shot is triggered

and produces a 15 m.s. blanking pulse. This pulse simultaneously blanks each controller (Figs. IV-7 and 8), and saturates the integration capacitors in the current limit loop. After the end of the blanking pulse, the capacitors discharge at a gradual rate which allows the duty cycle to slowly increase. The load current also increases at a gradual rate. If the short is still present the current limit will be activated before the current becomes excessive. In other words, the gradual current buildup prevents the high peak currents that might otherwise occur due to abrupt turn on after the blanking pulse. Fig. IV-3 shows that the Hall effect current sensor actually monitors the currents in the two L1 windings instead of the load current. This was found to provide more reliable transient protection, and the connection shown effectively rectifies the two currents for the sensor. I_{s1} could have been monitored instead, but since I_{s1} is bi-directional, a - 15 VDC supply would be needed for H1 along with a rectifier bridge at the H1 output.

6. Master and Slave PWM Controllers. These circuits are standard 494 PWM controllers whose schematics are shown in Figs IV-7 and 8. A2 and A3 are slaved to A1 so that all three operate in synchronism at the same frequency. In spite of all of the isolation precautions (optical coupling, Hall effect devices, and the isolation amplifier), some interference between the three controllers occurred initially. This interference persisted on a random basis until the three controllers were moved to a distance of about 3 ft. from the converter modules. Apparently, the slight differences in the three duty cycles create noise that generates logic errors in the controllers. This indicates that similar problems may occur in any high power system consisting of parallel modules unless the modules are packaged individually for low EMI.

7. Logic Power Supply. This circuit is shown in Fig. IV-9.

Test Data for a Single 900 Watt Converter.

1. Efficiency:

Tests were initially performed on a single converter operating at 20 kHz. Efficiency measurements were performed by measuring the DC input and output voltages and currents with calibrated digital meters:

f = 20 kHz.

V_{IN} = 115.1 Vdc, I_{IN} = 8.91 Adc

V_o = 410 Vdc (only 3 digit accuracy above 200 V.), I_o = 2.20 Adc

Efficiency = 88%.

In an effort to increase the efficiency, the frequency was lowered to 10 kHz. This produced significant audible noise, but this was not considered to be a serious problem since the converter is not intended for locations where personnel will be present for long periods of time. It also is quite likely that spacecraft versions of this circuit would use a Ni-Fe core for T1 because of the fragile nature of ferrite cores. If this is the case, previous studies [5] have shown that a 10 kHz design does not represent a major weight increase over 20 kHz. The efficiency was then measured in the same manner as before:

f = 10 kHz.

V_{IN} = 115.0 Vdc, I_{IN} = 8.58 Adc,

V_o = 410 Vdc, I_o = 2.20 Adc

Efficiency = 91.4%

Because of this significant increase in the efficiency, it was decided to operate at 10 kHz.

2. Voltage Regulation:

Load regulation test results are as follows:

I_o	0	0.5	1.0	1.5	2.0	2.2	Adc
V_o	410	410	410	410	410	410	Vdc

3. Waveforms:

Figs. IV-10-14 slow various waveforms that were obtained with a Tektronix 11401 digitizing oscilloscope. Fig. IV-10 shows v_{CE} and i_E for Q1 where the v_{CE} trace indicates the relatively high v_{CE} transient of ~400 volts that occurs at Q2 turn off, even though V_{IN} is only 115 Vdc. The currents in the primary and secondary of L are shown in Fig. IV-11.

Transistor energy loss measurements can be obtained from the following information:

Turn-on energy loss from Fig. IV-12:

$$E_{on} = \int_0^{t_{on}} (v_{CE1}(t) \times i_{Q1}(t))\, dt$$

Conduction energy loss for from Fig. IV-13:

$$E_{cond.} = \int_0^{t_{con}} (v_{CE1}(t) \times i_{Q1}(t))\, dt$$

Turn-off energy loss from Fig. IV-14:

$$E_{off} = \int_0^{t_{off}} (v_{CE1}(t) \times i_{Q1}(t))\, dt$$

A convenient way to obtain these area measurements is to use the Area (-) calculation that is available on the Tektronix 11401 digital scope. The oscilloscope first calculates the $(v_{CEI} \times i_{Q1})$ waveform and then measures the area under this curve for the three time intervals. If the curve has areas above and below the zero reference level, Area (-) is calculated as follows:

Net Energy in = Area (-) ≡ (Area above) - (Area below)

This should correspond to the net energy dissipation since (Area above) represents energy flowing into the switch while (Area below) represents energy flowing out. In this case (Area below) should be zero since energy only flows into

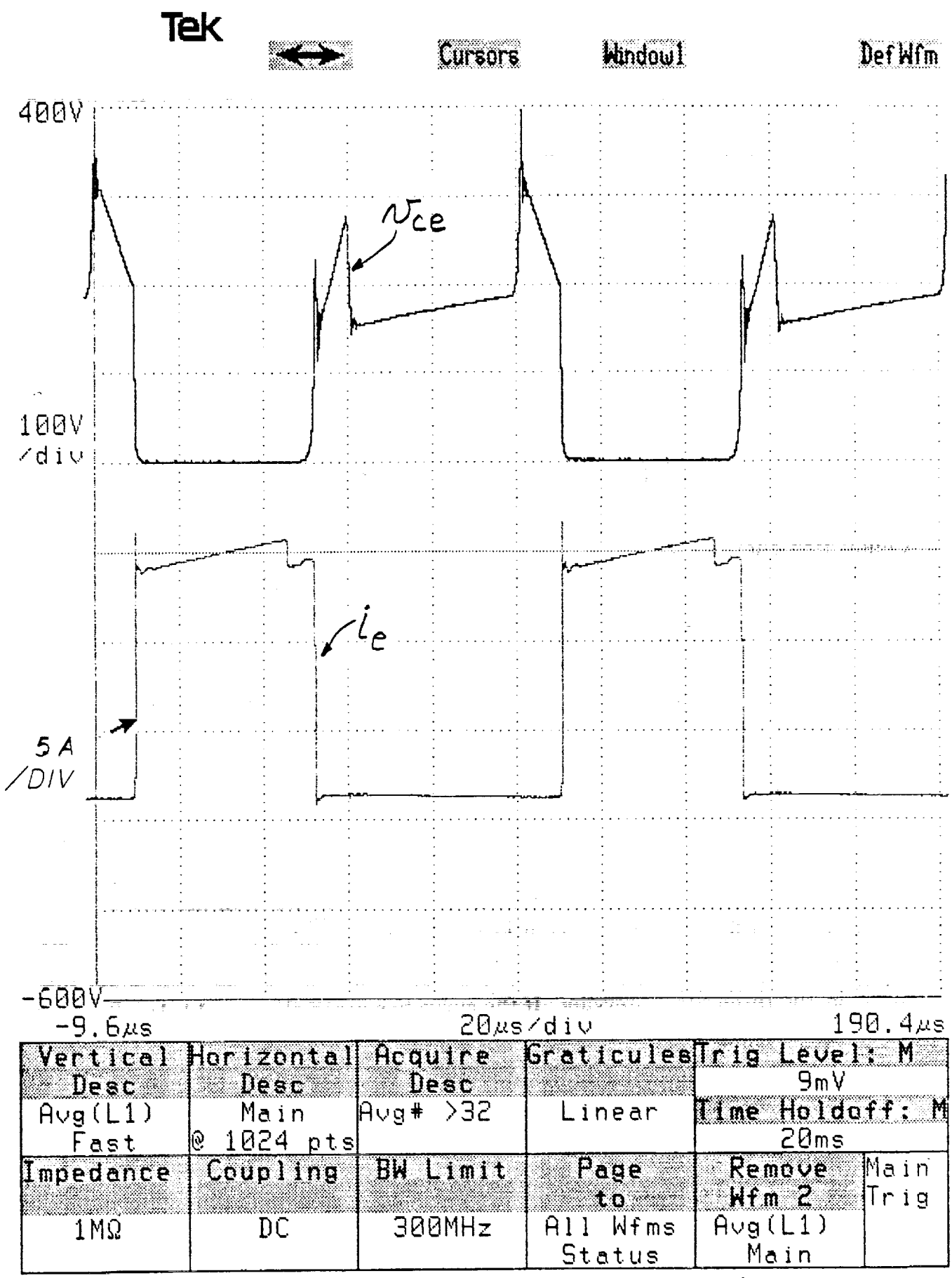


Fig. IV-10. v_{ce} and i_e for Q1.

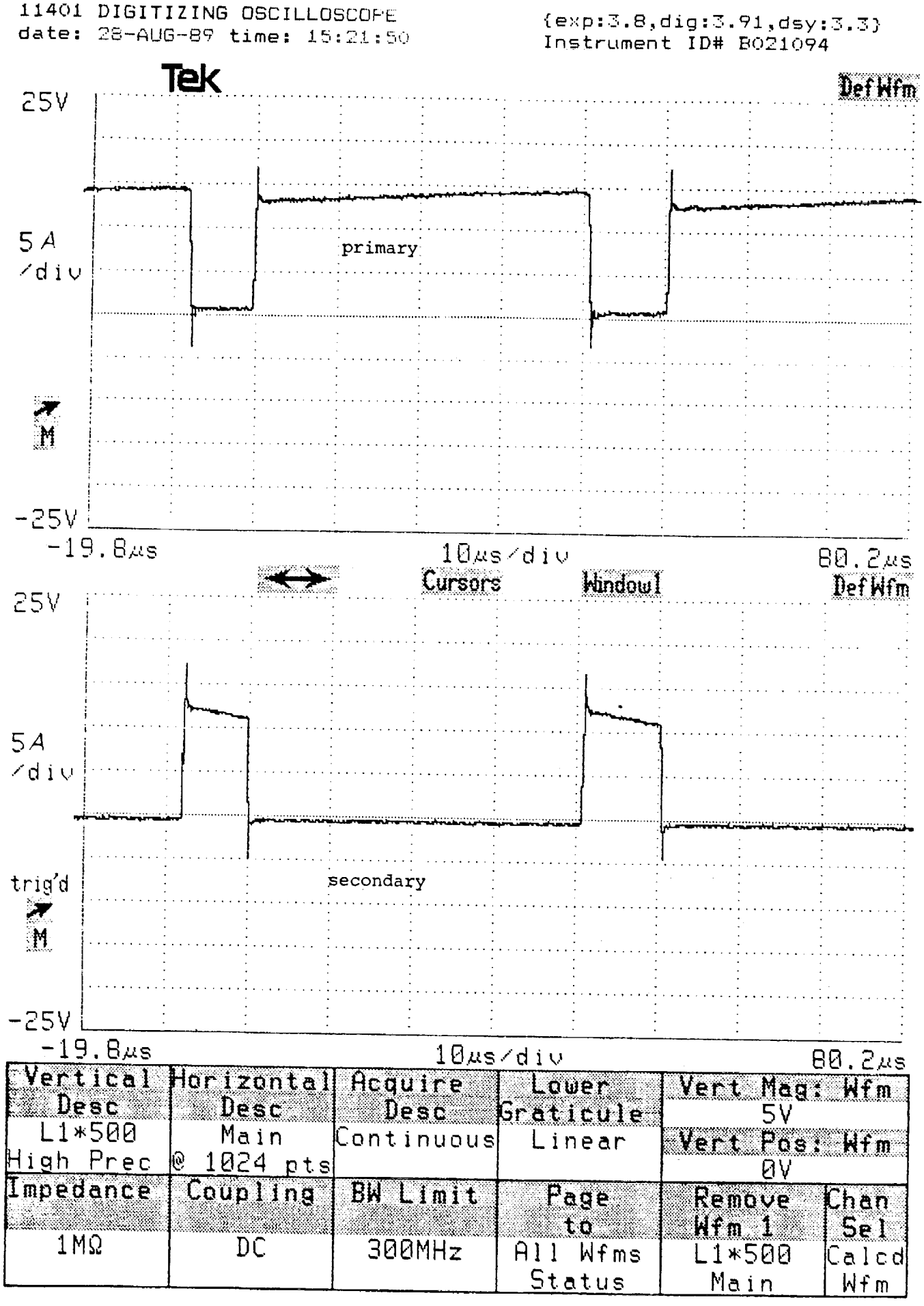


Fig. IV-11. Primary and secondary currents in L.

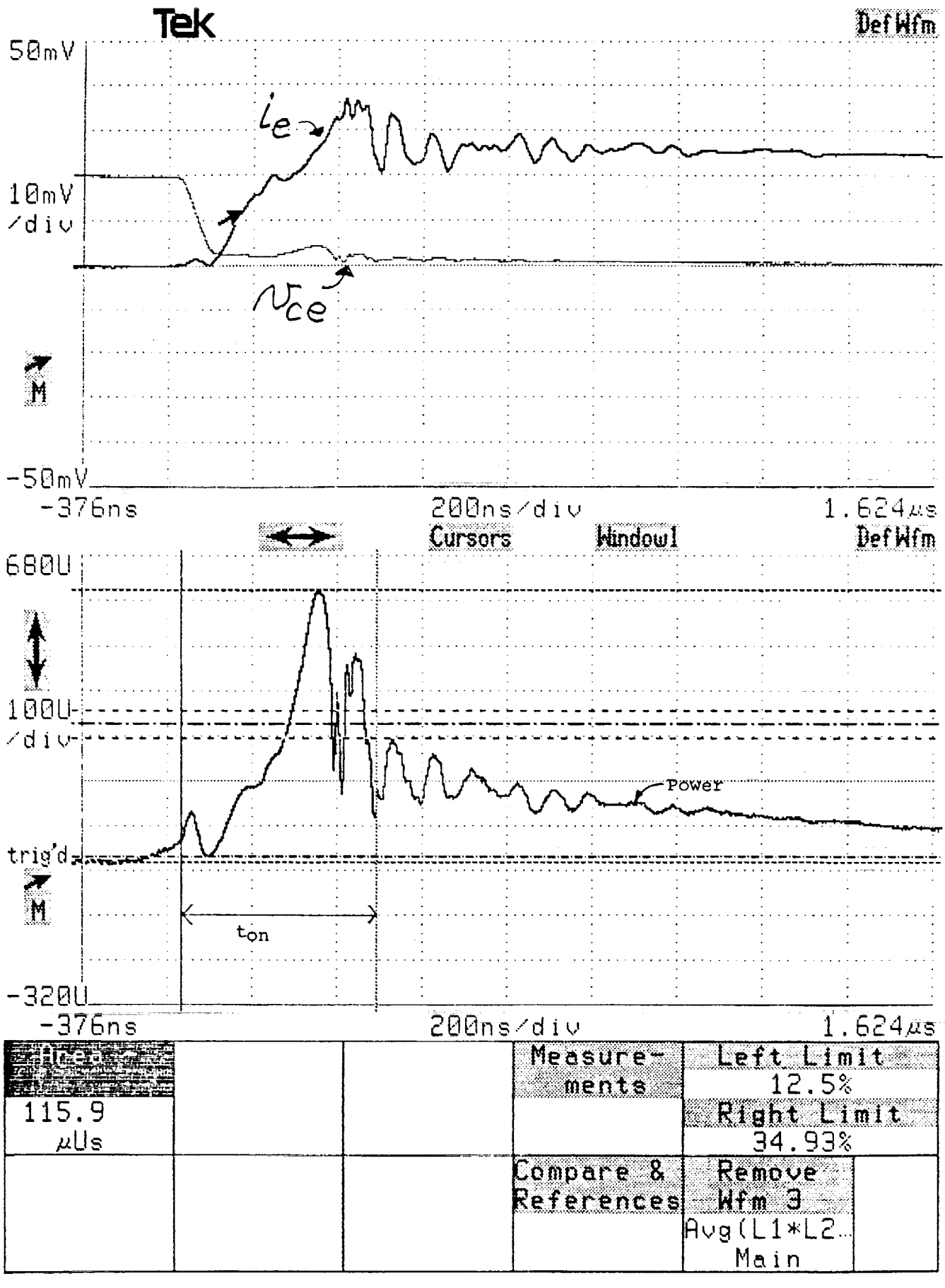


Fig. IV-12. Energy loss during turn-on interval.

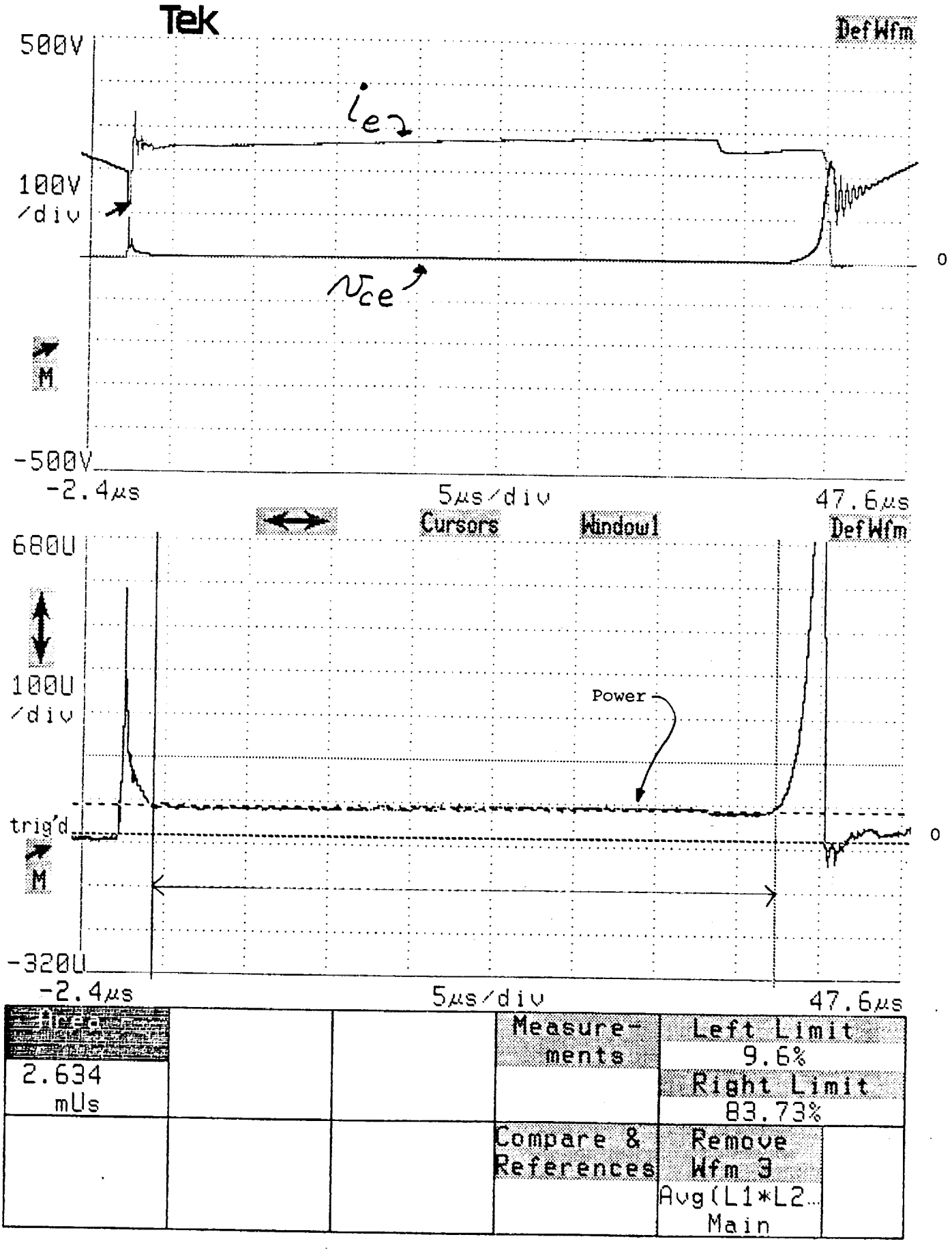


Fig. IV-13. Energy loss during conduction interval.

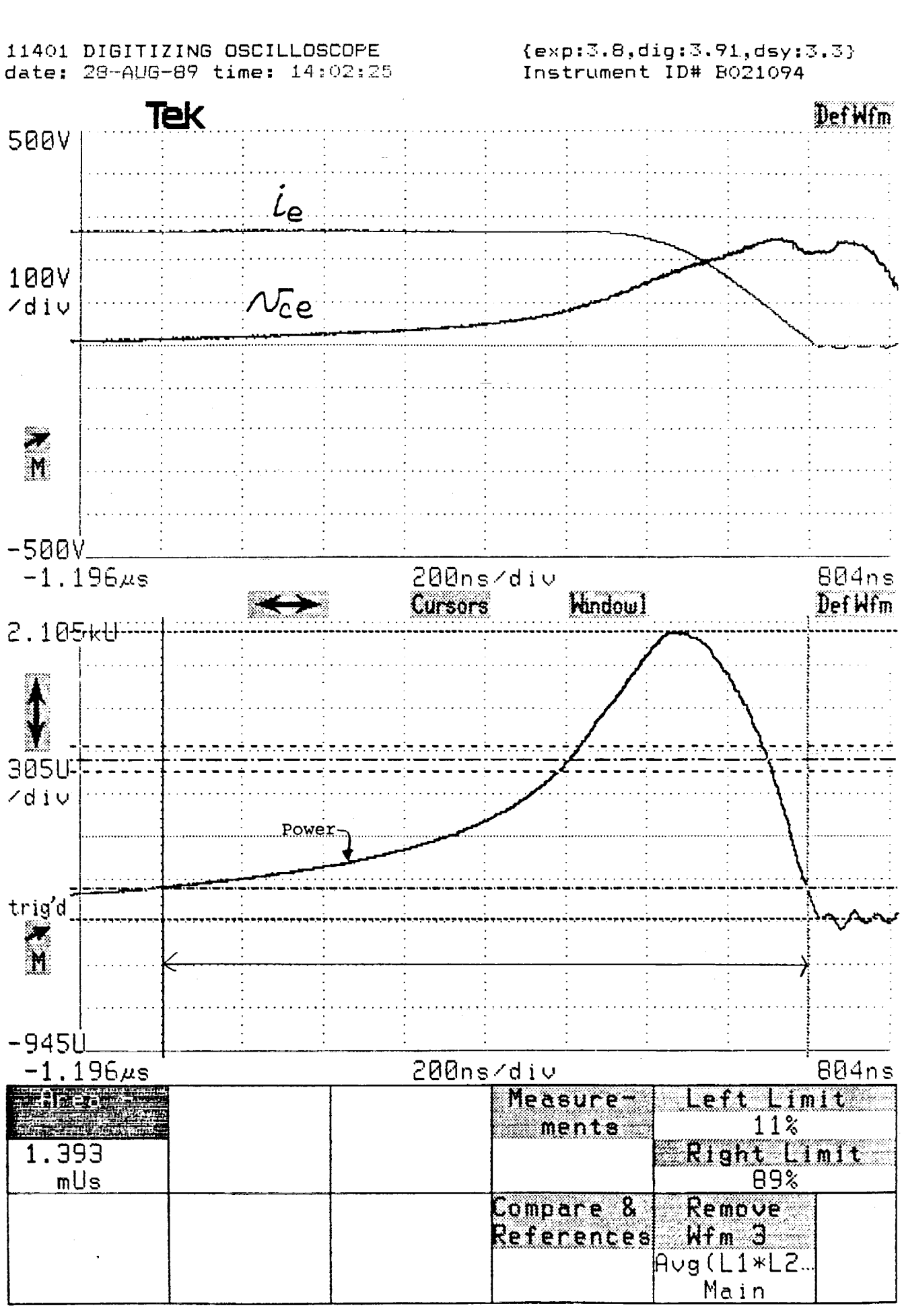


Fig. IV-14. Energy loss during turn-off interval.

the switch.

Another problem that must be considered is the proper scaling factor for the Area (-) calculation. This factor is obtained in the following manner:

Current probe: $\left(\frac{5\text{ A.}}{10\text{ mV.}}\right) = 500$ A./V.

Voltage probe: 1:1

$\therefore$ Scale factor = SF = 1 x 500 = 500

Thus if Channel 1 (V1) is connected to the current probe and Channel 2 (V2) is connected to the voltage probe, the scope is programmed to perform the following calculation,

$$(v_{CEI} \times i_{Q1}) = V1 * V2 * 500$$

The vertical scale on the product waveform (lower trace of Figs. IV-12-14) will then be,

1 U = 1 watt

so the trace indicates instantaneous power vs. time.

The area (-) calculations will be in Joules. On the scope these units are designated as Us, where in this case, 1 Joule = 1 Us. Figs. IV-12-14 indicate the losses are as follows:

Turn-on loss = 115.9×10^{-6} J. (Fig. IV-12)

Conduction loss = 2.634×10^{-3} J. (Fig. IV-13)

Turn-off loss = 1.393×10^{-3} J. (Fig. IV-14)

To obtain repeatable results, it is necessary to define the boundaries of t_{ON}, tcon, and t_{OFF}. Ton and t_{OFF} were defined in the following manner:

t_{ON}, t_{OFF} = interval where $v_{CE1} \times i_{e1} > 0.1\ v_{CE1} \times i_{E1(max.)}$

The beginning and end of the conduction interval tend to be fairly distinct points, so these were used to define t_{con}, as indicated in Fig. IV-13.

Measurements of switching and conduction losses become quite useful for estimating total transistor losses at different operating frequencies. Energy losses such as those in Figs. IV-12-14 can be converted to average power loss in the following manner:

$$P_{loss} = \frac{E_{on} + E_{con} + E_{off}}{T}$$, where T = period

For the losses in Figs. IV-12-14 at 10 kHz,

$$P_{loss} = \frac{(.116 + 2.63 + 1.39) \times 10^{-3}}{0.1 \times 10^{-3}} = 41.4 \text{ watts @ } 10 \text{ kHz}.$$

If the frequency is increased to 20 kHz., one would expect the switching energy losses to be about the same, but the conduction energy loss should decrease by 50% because of the 50% decrease in the conduction time. Therefore for 20 kHz,

$$P_{loss} = \frac{(.116 + 1.39 + 0.5 \times 2.63) \times 10^{-3}}{.05 \times 10^{-3}} = 56.4 \text{ watts @ } 20 \text{ kHz}.$$

Therefore, at 20 kHz the total increase in the loss for both transistors would be,

$$\text{Estimated } \Delta P_{Q1,\,Q2} = 2(56.4 - 41.4) = 30.0 \text{ watts}$$

Transistor loss measurements were not performed when the circuit was originally operated at 20 kHz, but the overall measured efficiencies and losses at both frequencies were,

Frequency	Efficiency	Total Loss
10 kHz.	91.4%	84.7 watts
20 kHz.	88%	123.54 watts

$\therefore$ Total measured $\Delta P = 123.54 - 84.7 = 38.84$ watts

This result seems quite reasonable in light of the fact that losses in the other components such as the magnetics will also increase with increasing frequency.

4. Stability Analysis:

As derived in Section II, the open loop voltage gain transfer function for the PPCF converter is of the form,

$$G_{(s)} H_{(s)v} = \frac{V_1 K_{1(s)} H_1 \left[1 + \frac{s(2D_1 - 1)L}{D_1^2 R}\right]}{V_p D_1^2 \left[\frac{s^2 LC}{D_1^2} + \frac{Ls}{RD_1^2} + 1\right]} \qquad \text{(II-52)}$$

If a simple integrator of the form,

$$K_{1\,(s)} = \frac{K_v}{R_1 C_1 s}$$

is used, (II-52) indicates that the system should be easy to stabilize if R_1C_1 is large enough (lag compensation). This is verified by the gain-phase plots in Figs. IV-15 and 16 for full and light loads, respectively. The maximum phase shift in Fig. IV-15 is considerably less than that in Fig. IV-16 because the zero in (II-52) is well above the measured frequency range for large values of load resistance, R.

Although the plots in Figs. IV-15 and 16 indicate a stable system, the transient response of the converter may be rather slow because the 0 db point is only at about 100 Hz. If the integration capacitor, C_1 = .033 μfd., decreased, a wider bandwidth and faster transient response would result. This is shown by the plot in Fig. IV-17 where C_1 has been decreased to .0033 μfd to increase the 0 db point to almost 1000 Hz. However, this system depends on the zero in (II-52) to prevent 180° phase shift before the 0 db crossing point. For large values of load resistance, R, this zero may become too high to provide adequate compensation. This is indeed the case with the present circuit, and for C_1 = .0033 μfd, the system becomes unstable for $I_L \leq 0.57$ Adc.

A more extreme example of this bandwidth-stability trade-off is shown in Fig. IV-18 where C_1 = .001 μfd. In this case the 0 db point has increased to 2 kHz, but the system becomes unstable for $I_L \leq 1.5$ Adc.

In spite of the low bandwidth, the final system used C_1 = .033 μfd in order to provide large gain and phase margins. No gain or phase measurements were taken with the three converter modules operating in parallel since no method has yet been found for measuring the stability of such a system (see Section III). No stability problems were experienced with all three modules in parallel however.

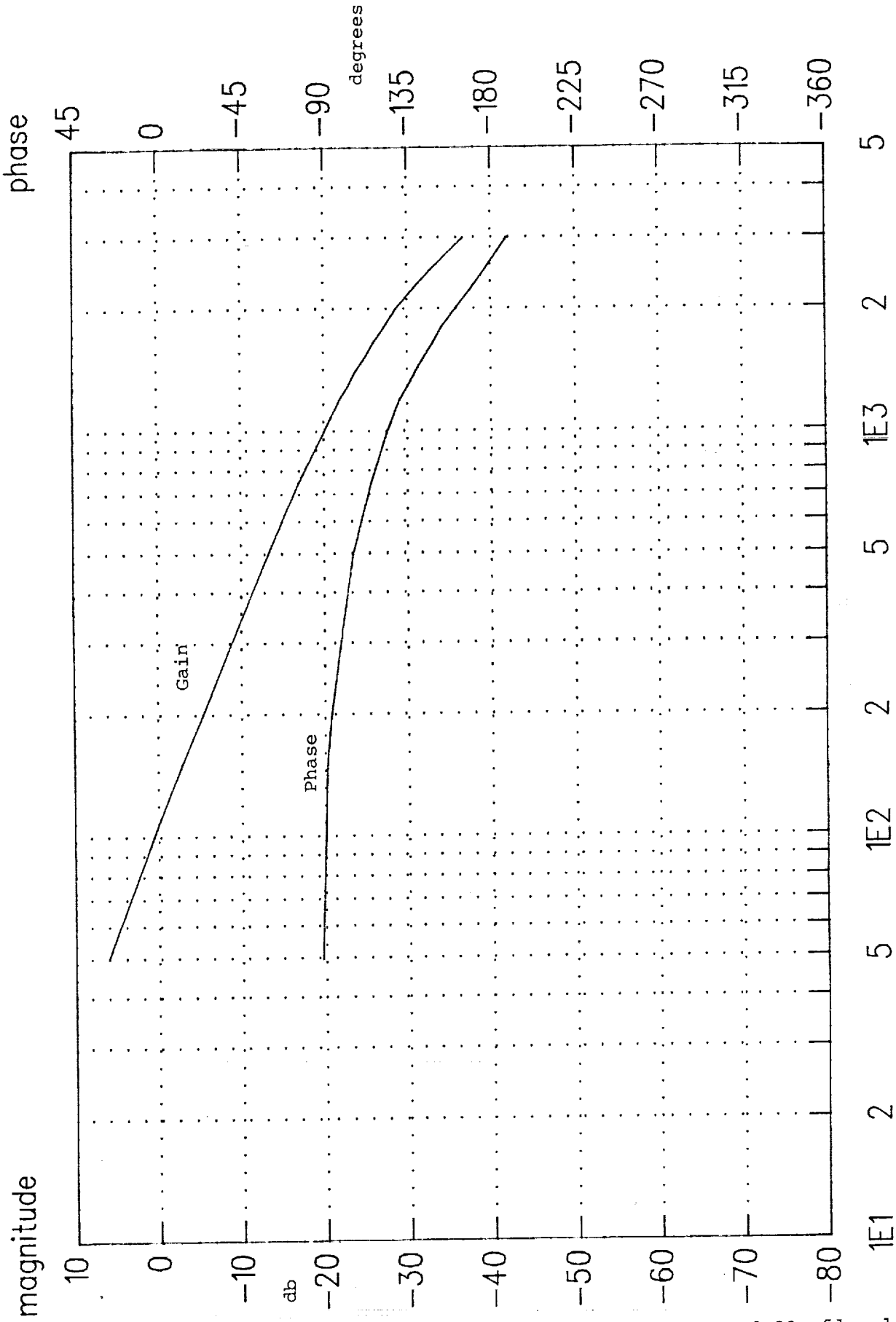


Fig. IV-15. Open loop voltage gain and phase shift for C_1 = 0.33 µfd and I_L = 2.2 Adc.

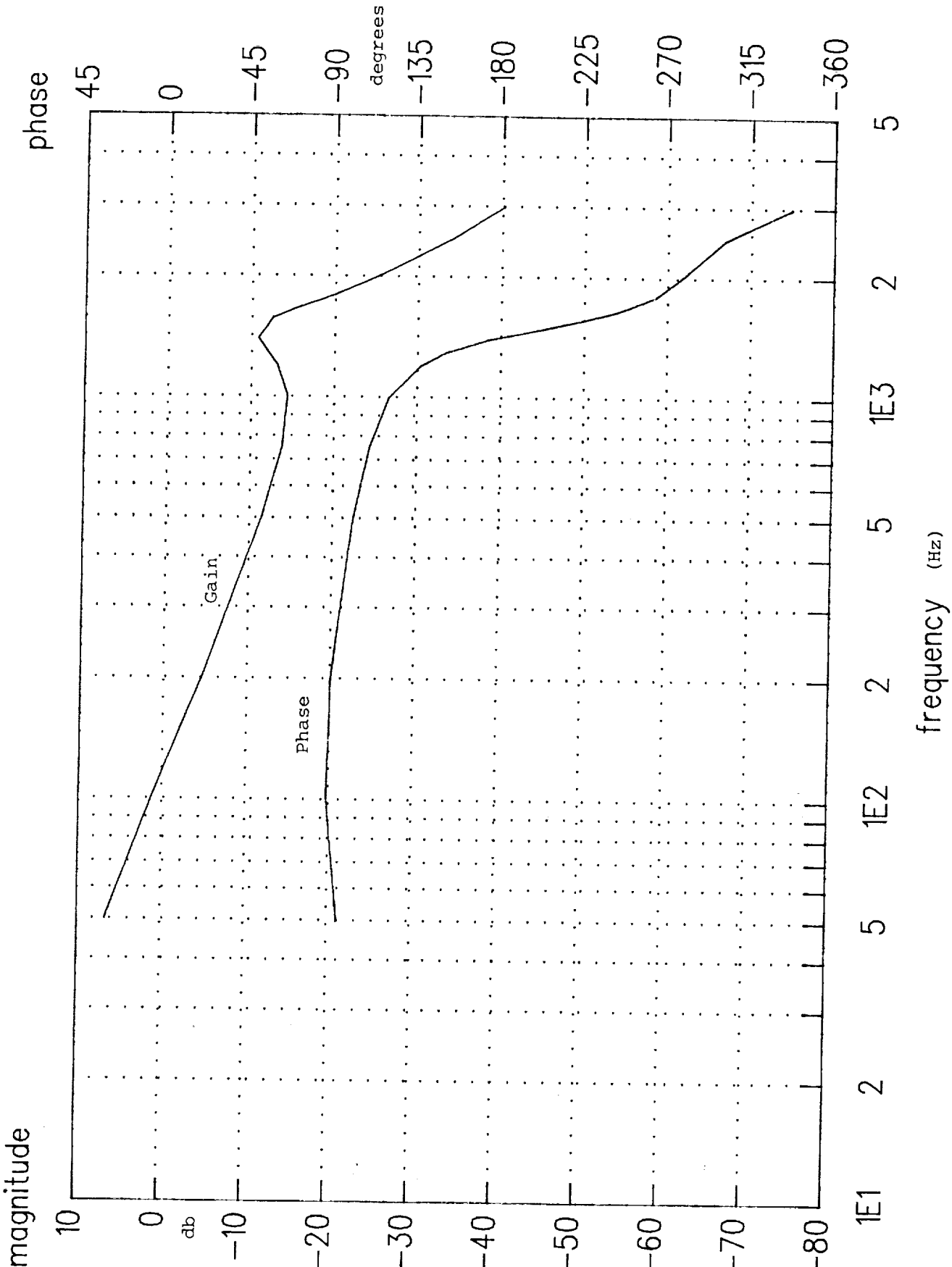


Fig. IV-16. Open loop voltage gain and phase shift for C_1 = .033 µfd and I_L = 0.11 Adc.

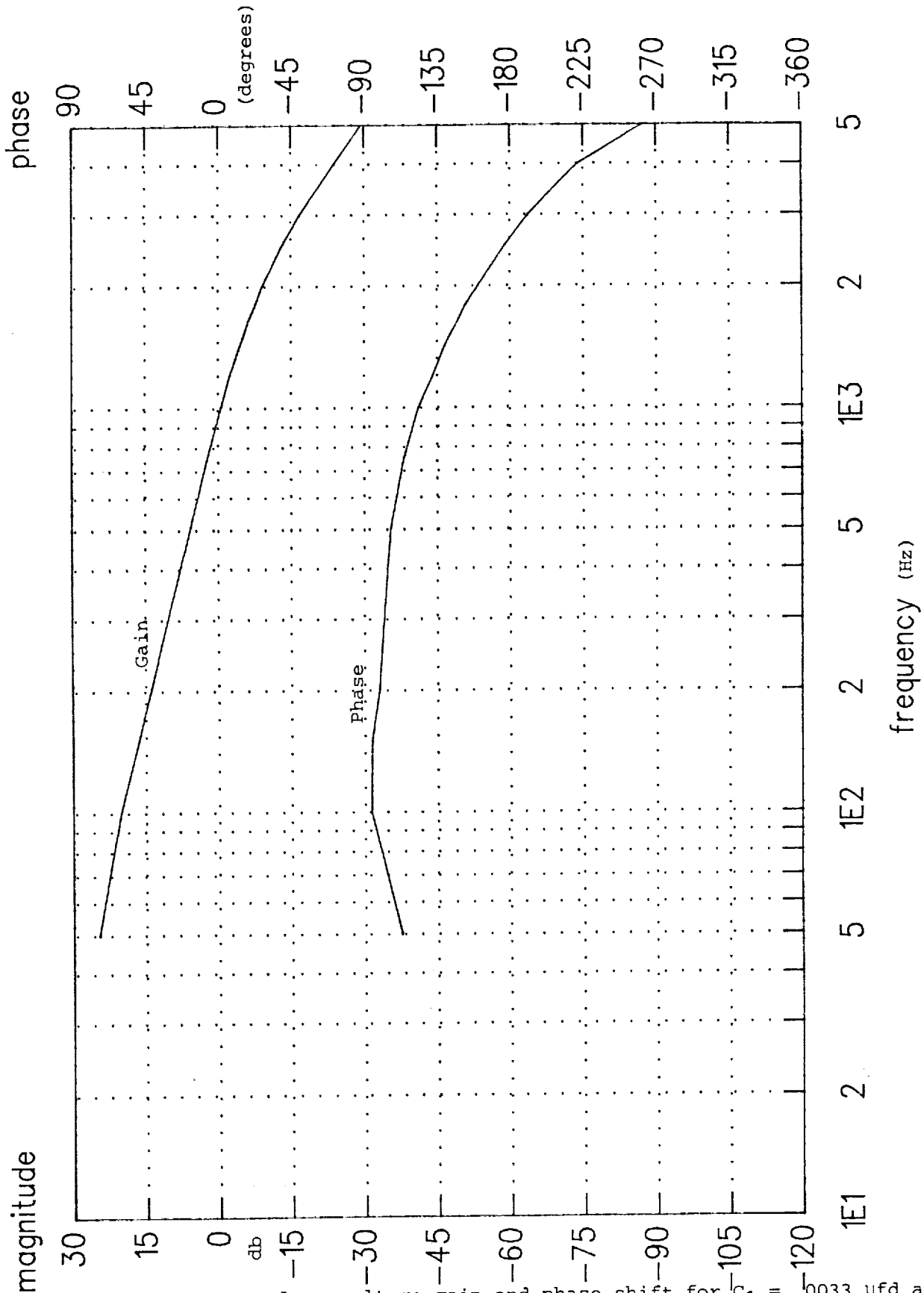


Fig. IV-17. Open loop voltage gain and phase shift for C_1 = .0033 µfd and I_L = 2.2 Adc. System is unstable for $I_L \leq$ 0.57 Adc.

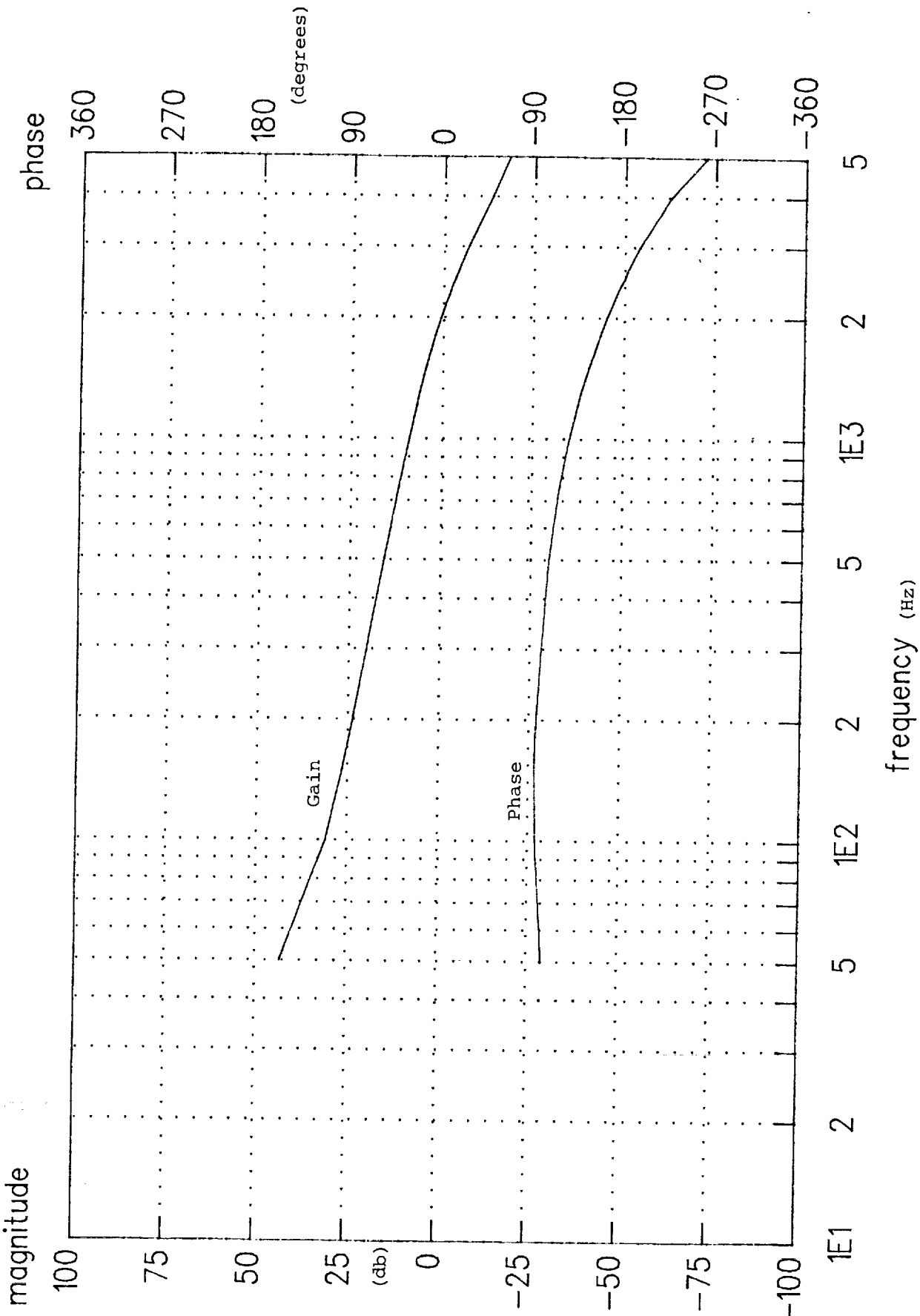


Fig. IV-18. Open loop voltage gain and phase shift for C_1 = .001 µfd and I_L = 2.2 Adc. System is unstable for $I_L \leq$ 1.5 Adc.

5. Short Circuit Tests

All three modules were tested extensively by applying an abrupt short circuit across the output. No failures were experienced once the final short circuit protection design was established. Test results are shown in the experimental results for all three modules in parallel since this is considered to be the most severe test.

Test Data for Three Converters in Parallel

1. Efficiency:

Efficiency tests were performed at 10 kHz in the same manner as for the single converter tests:

f = 10 kHz

V_{IN} = 115.0 Vdc, I_{IN} = 25.6 Adc, V_o = 409 Vdc, I_o = 6.56 Adc

Efficiency = 91.1%

Load regulation test results are indicated below. As expected, the voltage variation is slightly greater than for the single converter case. This is because each converter regulates the voltage over a different portion of the load range, and the voltage calibration points are slightly different for each of the converters.

I_o	0	1.0	2.0	3.0	4.0	5.0	6.0	6.6	Adc
V_o	411	411	411	410	410	409	409	409	Vdc

2. Short Circuit Test:

The system was tested extensively by applying an abrupt short circuit while operating at a full 2700 watt load. No failures were experienced during any of these tests. As indicated in the section describing the short circuit protection, there are actually two current limit circuits, one for steady state and one for transients. The steady state limiter is absolutely necessary for parallel operation, and the transient limiter is a safety precaution to provide a much faster response time than that of

the steady state limiter.

Fig. IV-19 shows the current entering the center top of each transformer primary for a 2700 watt load. Phase C is regulating the voltage while phases a and b are in steady state current limit. Fig. IV-20 shows the same waveforms during the transient current limit mode with a short circuit across the output. The transient current limiter operates in the following sequence:

1. All three converters are turned off immediately if the transient current limit is exceeded in any of the three.
2. All three converters are held off for 15 M. S.
3. The currents are allowed to ramp up at a gradual rate.
4. If any of the three transients limits are exceeded during the ramp, the sequence repeats.

For Fig. IV-20, the transient limits were set so that the limit cycle will continue to repeat for a short circuit. If the time scale was increased, one would observe an approximate series of 2 ms current bursts 15 ms apart. This waveform was not included because the sampling rate of the digital scope is too low to properly display each burst for this longer time scale. However, the waveform is easily obtained on a conventional scope. Fig. IV-21 shows an expanded view to indicate each current pulse in greater detail.

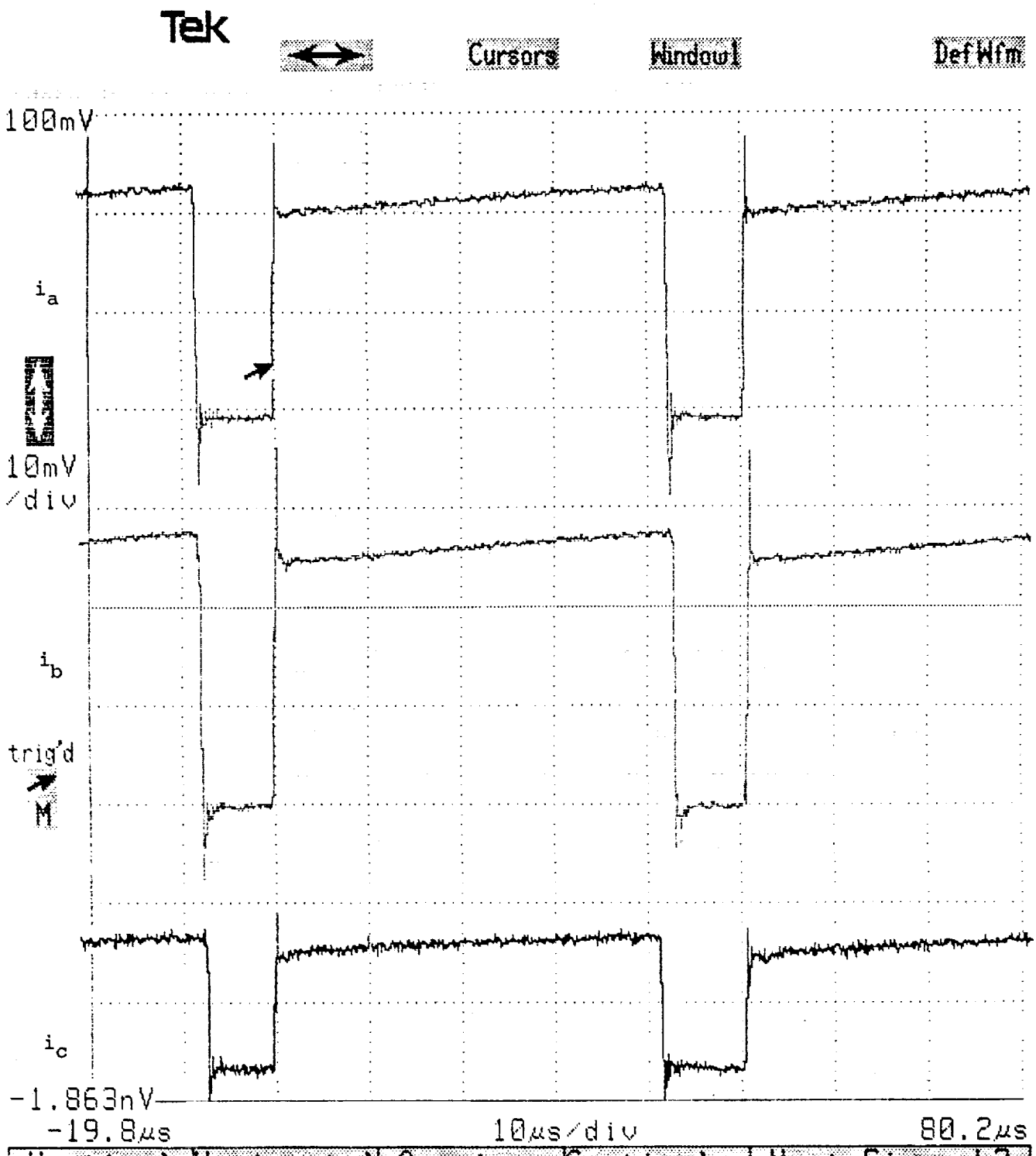


Fig. IV-19. Center tap current waveforms for 2700 watt load.

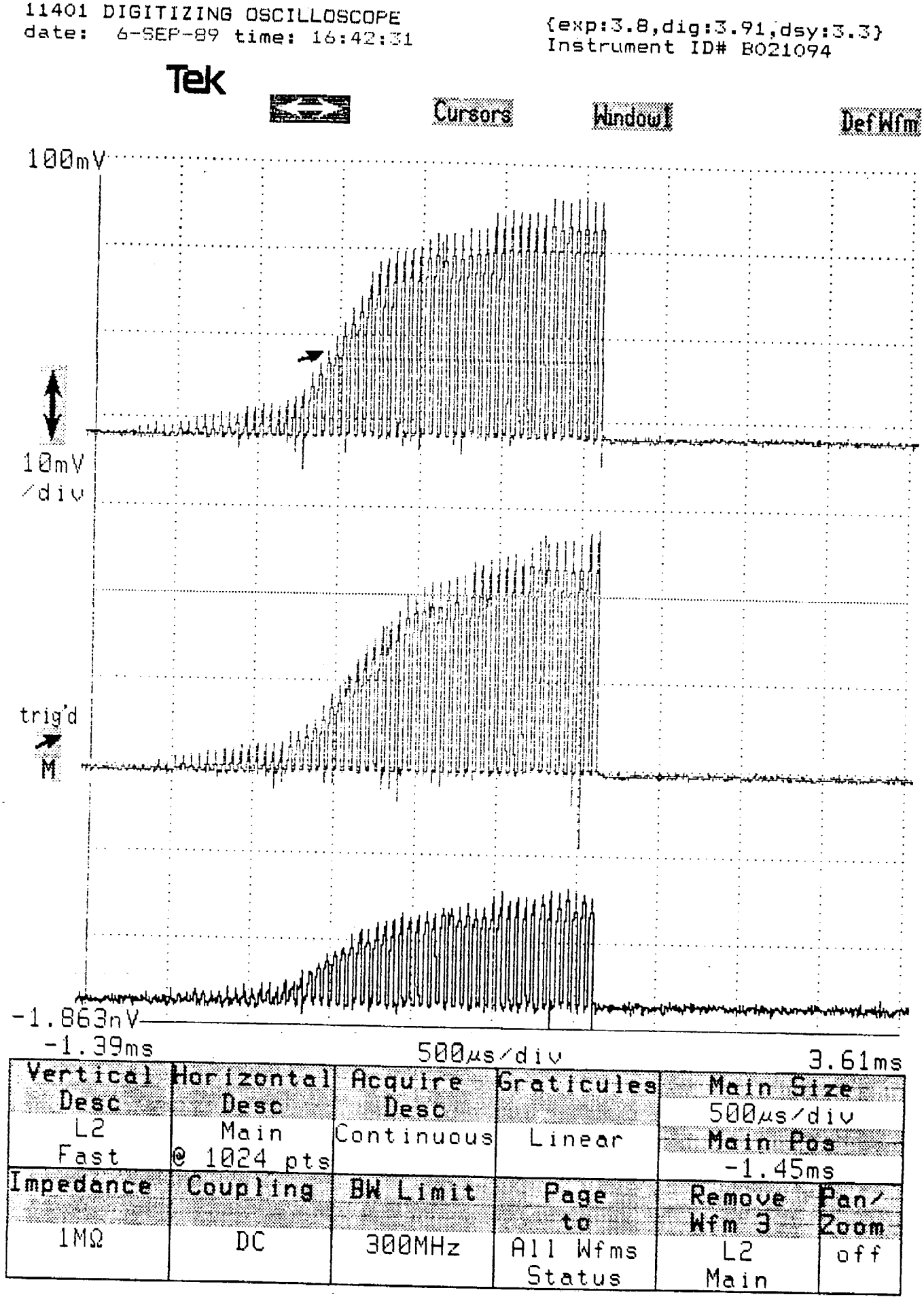


Fig. IV-20. Center tap current waveforms during transient current limit, V_o= 0 Vdc.

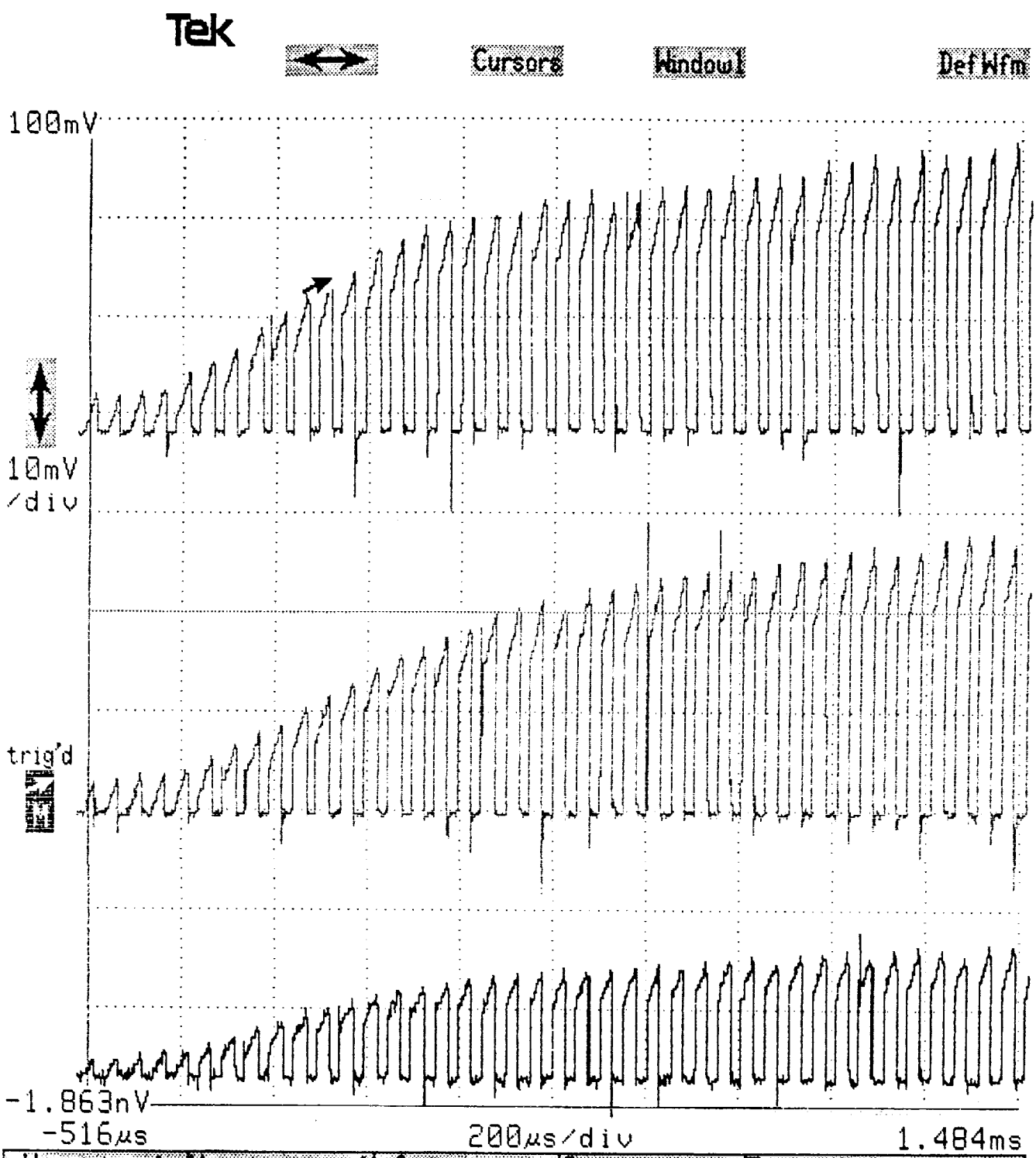


Fig. IV-21. Expanded display of center tap waveforms shown in Fig. IV-20.

V. SHUNT REGULATOR FOR THERMOELECTRIC CONVERTER

Shunt Regulator Design

The design of an appropriate shunt regulator will be driven primarily by the following factors:

1. The need for high "efficiency" in a 120°C environment.
2. The tradeoff between a high-radiation design and high shielding mass.
3. The need to provide low output impedance over a given frequency band.
4. Requirements for modularity (with redundancy) and a means of isolating a faulty module.

Item 1 is not initially apparent, because the purpose of the shunt regulator is the dissipation of unneeded power. However, the system mass will be strongly affected by the portion of power dissipated as switching and conduction losses on the 120°C baseplate. This is so because the ballast resistors can be operated at a high temperature with a small radiator, while the low-temperature (120°C) radiator is dramatically larger. For example, if the ballast radiator is operated at 800°C, and the background temperature is assumed to be 273°K, the low-temperature radiator would require an area 72 times that of the high-temperature radiator for a given power. The "efficiency" of the shunt regulator is therefore defined to be

$$\eta \equiv \frac{\text{power dissipated at high temperature}}{\text{total power dissipated}} \qquad \text{(V-1)}$$

Care should be taken in the design of the shunt regulator to maximize η. This can be done by keeping switching-device conduction and switching losses as low as possible.

Item 2 recognizes the fact that a thermoelectric system will produce electricity at a low voltage level (100-200 V). Transmission and distribution at this voltage level will necessarily require a high cable mass, so it is likely that power processing in the vicinity of the thermoelectric heat source will be required. This

heat source is assumed to be nuclear, thus a trade-off needs to be made between radiation shielding mass and radiation-tolerant design of the shunt regulator (and other power-processing equipment). This trade-off is complicated by the fact that radiation-tolerant switching devices tend to have higher conduction losses, thus increasing the mass of the low-temperature radiator. It is apparent that there are at least three interacting factors to be considered: 1) cable mass, 2) shielding mass and 3) low-temperature radiator mass. Proper consideration of these alternatives will require the characterization of the switching and conduction losses of suitable devices in a high-radiation environment. This work is yet ongoing; therefore, this trade-off was not considered further.

Item 3 is one of the key specifications of any constant-voltage power source. For small load-current perturbations, the shunt regulator output inpedance characterizes the interaction between the regulator and its load. Because the loads themselves will primarily be switching regulators, this small-signal output impedance will affect the design and compensation of the switching regulator control loops and input filters. In addition to a small-signal impedance specification, there will also be transient output voltage limits for large load current changes. These large-and small-signal specifications will determine the minimum shunt-regulator switching frequency, bypass capacitor value and control-loop design.

Item 4 is primarily motivated by concerns for reliability and the use of an optimum module size to construct a large system. However, it will be seen that there is also a trade-off possible among the number of modules, switching frequency and output bypass capacitor size.

The experimental 2.5 kW shunt regulator was designed making an effort to achieve low switching and conduction losses at 120°C. A state-space-averaged large-signal (nonlinear) model was derived for the purpose of studying the large- and small-signal output impedance characteristics. The shunt regulator was implemented using three modules, any two of which provided full-power operation. A controller which could automatically work around a failed module was demon-

strated in the experimental hardware. Experimental data were taken verifying these analytical results.

Proposed Switching Strategies

The proposed module arrangement is illustrated in Fig. V-1. The thermoelectric converter is represented by its open-circuit voltage V_{int} and its internal resistance R_{int}. Assuming maximum-power-transfer operation, the nominal value of v_o will be one-half V_{int}, and shunt resistor sections having a combined value of R_{int} must be available for proper operation. Setting R equal to R_{int}, N sections are required: N + M sections are shown, providing M spare shunt sections.

The redundancy provided by the extra shunt sections improves the reliability. An open-circuit failure of a ballast resistor can be compensated by "tagging" the faulted unit and activating one of the spares in its place.

The most likely failure mode would be short-circuit of a switching device. Operation could continue at reduced output rating in this case by omitting the drive signal for the faulted unit and reprogramming the controller for N-1 switches (to prevent a dead zone from appearing in its transfer characteristic). If a one-time circuit interrupter (such as an explosive link) were provided to remove a faulty shunt section, then full-power operation could be restored.

Three possible switching strategies were identified: 1) step-wise (discrete) control of v_o, 2) individual pulse-width-modulation (PWM) control of the switches, with N progressive phase displacements, and 3) one master controller providing discrete control of N-1 switches with PWM control of the Nth switch. The discrete control requires only a single controller making a quantized decision concerning the number of switches to close or open to minimize the output voltage error. This would be simple to implement using digital hardware and, in the steady state, would incur no switching losses at all. The main disadvantage would be the quantized nature of the available output voltage values. This method could only work with a large number of switches and a loose tolerance on the output voltage. An additional disadvantage would be a high incremental output impedance

because no output voltage feedback could take place, except in discrete steps.

The second method considered, progressively-phase-displaced PWM, is attractive because of its high degree of redundancy (each switch has its own controller which could operate independently). The progressive phase displacement permits a much smaller output capacitor C_o due to cancellation of the first N-1 harmonics of the switching frequency in the output ripple. The operation of this switching strategy is illustrated in Fig. V-2, which shows the switch existence functions (1=closed, o=open). The N controllers each apply the same duty cycle d, but with progressive phase displacements of $2\pi/N$. It will be shown in the next section that this progressive phase displacement reduces the switching-related ripple in the output. However, there would probably be some technical difficulty is maintaining sufficiently accurate phase displacement and section-to-section uniformity for large N. Also, the problem of resetting the phases of the individual PWM controllers after the removal of a faulty ballast section would have to be considered. Because a complete PWM controller is associated with each ballast section, they could be operated independently if necessary. The benefits of ripple cancellation would then be lost, however.

The third switching strategy considered, and the one implemented in the experimental hardware, combines the advantages of the previous two approaches. In this method, the controller applies discrete control to the first N-1 usable switches, and PWM control to the Nth switch. This approach has the advantage that N-1 switches incur no steady-state switching losses. The PWM control applied to the Nth switch maintains infinite-resolution control of the output voltage with low incremental output impedance. (The effective large-signal output impedance depends upon the rapidity with which the controller can change the states of large numbers of switches.) This "discrete/PWM" strategy was found to have lower switching losses and to be relatively easy to implement. Control of the redundant ballast sections was found to be especially straightforward. A more-detailed comparison of the three approaches considered here is made in the next section.

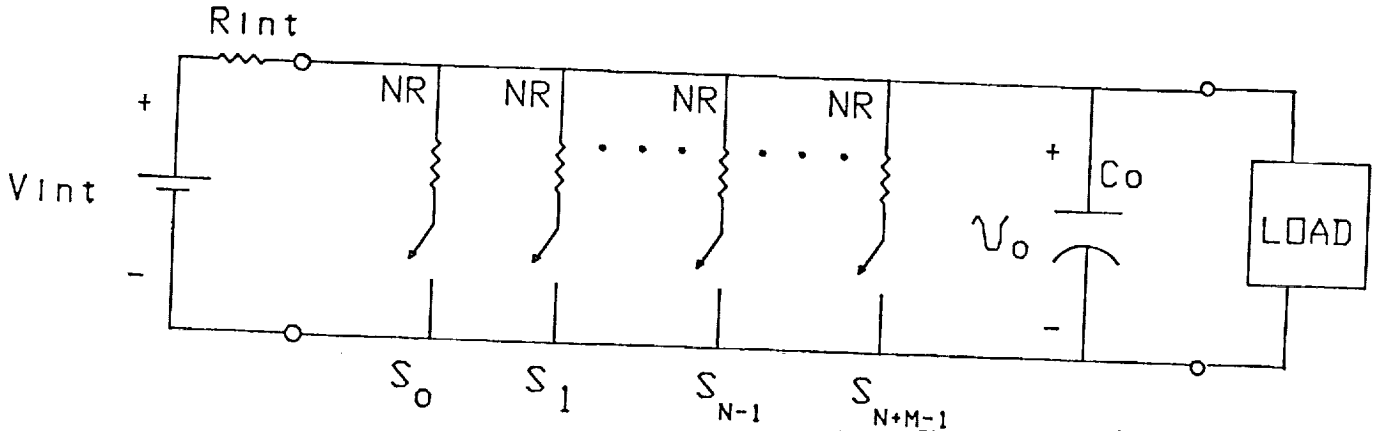


Fig. V-1. Proposed shunt regulator module arrangement.

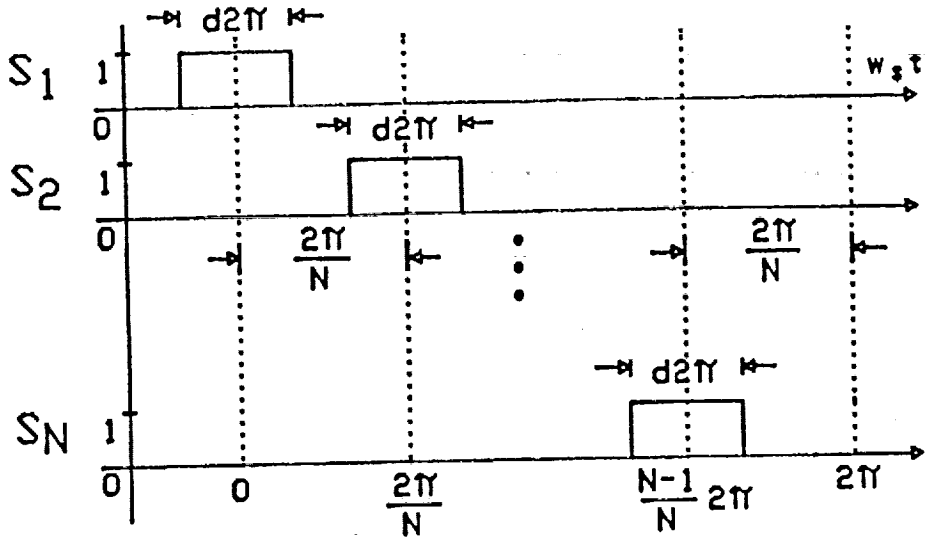


Fig. V-2. Switching existence functions for progressively-phase-displaced PWM.

Comparison of Three Switching Strategies

The first point of comparison to be made is the relationship among switching frequency, number of ballast sections and bypass capacitor size for each of the three switching strategies. The discrete control approach does not switch in the steady-state: its bypass capacitor (if used) is therefore sized to provide a sufficiently-low output impedance to the loads connected to it. The switching-related output voltage ripple of the progressively-phase-displaced PWM and discrete/PWM approaches is next estimated.

Assuming an output voltage ripple low relative to its dc value, the currents in the individual ballast resistor sections of the progressively-phase-displaced PWM ballast then have the waveforms of Fig. V-2, with amplitudes of V_o/NR. The Fourier-series expression for the current in switch S_o is:

$$i_{so} = \frac{V_o}{NR}\left[d + \frac{2}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \sin nd\pi \cos n\omega_s t \right]. \qquad \text{(V-2)}$$

The current in the kth switch is therefore

$$i_{sk} = \frac{V_o}{NR}\left[d + \frac{2}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \sin nd\pi \cos \left(n\omega_s t - nk\frac{2\pi}{N} \right) \right]. \qquad \text{(V-3)}$$

where $k = 0, 1, \ldots N\text{-}1$.

A conservative estimate of the switching-related ripple voltage is found by assuming that all of the ripple current passes through C_o. Summing the contribution of all N ballast sections:

$$i_R = \sum_{k=0}^{N-1} i_{sk} . \qquad \text{(V-4)}$$

Using (V-4), with the identity

$$\sum_{k=0}^{N-1} \cos \left(n\omega t - kn\frac{2\pi}{N} \right) = \begin{pmatrix} 0, n \neq pN \\ N \cos n\omega t, n = pN \end{pmatrix} \qquad \text{(V-5)}$$

where p is any integer, gives

$$i_R = \frac{V_o}{R}\left[d + \frac{2}{\pi}\sum_{p=1}^{\infty} \frac{1}{pN} \sin pNd\pi \cos pN\omega_s t \right]. \qquad \text{(V-6)}$$

The dominant harmonic in the output voltage is seen to be $N\omega_s$, due to the cancellation of the first N-1 harmonics appearing in the individual ballast section currents. The ripple voltage appearing across C_o is then found by multiplying phasor expressions for each harmonic component of the ripple current i_R by the corresponding harmonic impedance of C_o. The dominant component is the $N\omega_s$ component: its magnitude is given by

$$|V_R(N\omega_s)| = \frac{2\,V_o|\sin Nd\pi|}{\pi\, N^2 R\omega_s\, C_o}. \qquad \text{(V-7)}$$

This component maximizes at duty cycle values d such that

$$d = \frac{k}{2N}, \text{ k any integer.} \qquad \text{(V-8)}$$

The worst-case switching-related ripple component expected in the output voltage therefore has the magnitude:

$$|V_R| = \frac{2\,V_o}{\pi\, N^2 R\omega_s C_o} V_{peak}. \qquad \text{(V-9)}$$

Thus there is a trade-off among switching frequency, number of shunt sections and the size of C_o for a given ripple requirement.

The discrete/PWM approach is next considered. In this strategy, only one shunt section is switching cyclically in the steady-state; therefore, the ripple voltage is found using (V-2) and the harmonic impedance of C_o. The resulting dominant component is at the switching frequency ω_s:

$$|V_R(\omega_s)| = \frac{2\,V_o|\sin d\pi|}{\pi\, N\, R\, \omega_s\, C_o}. \qquad \text{(V-10)}$$

The magnitude of (III-10) maximizes at d = 0.5, giving a worst-case ripple-component magnitude of

$$|V_R| = \frac{2\,V_o}{\pi\,N\,R\,\omega_s\,C_o}\,V_{peak}\,. \qquad \text{(V-11)}$$

Comparison of (V-9) and (V-11) shows that for a given switching frequency and number of shunt sections, the progressively-phase-displaced PWM requires a smaller (by a factor of N) bypass capacitor than does the discrete/PWM hybrid strategy.

The next comparison is made in the area of expected switch conduction loss. The following nomenclature is introduced:

d = duty cycle of a given switch, $0 \le d \le 1$

E_{SW} = switching energy loss (per switch)

N = number of ballast sections needed for normal operation

P_{COND} = total switch conduction loss

P_O = total rated output power

P_{SW} = total switching loss

R_{SW} = switch resistance (per switch)

V_{SW} = switch voltage drop

x = fractional ballast current, $0 \le x \le 1$

The conduction loss is estimated using the average switch current, if constant-voltage-drop is assumed, or the rms switch current, if resistive characteristics are assumed. In the discrete strategy, the integer number of the N available switches which best approximates xN will be closed. (The variable x is the fraction of the maximum ballast current which is currently required.) Therefore, the total conduction loss in the discrete strategy is

$$P_{COND} = (xN)\left(\frac{V_o}{NR}\right)(V_{sw}) = x\,\frac{V_{sw}}{V_o}\,\frac{V_o^2}{R}\,, \qquad \text{(V-12)}$$

assuming constant-voltage-drop switches. Normalizing conduction losses with respect to the rated output power, (V-12) becomes

$$\frac{P_{COND}}{P_o} = x \frac{V_{sw}}{V_o} . \qquad \text{(V-13)}$$

If resistive switches are assumed, the conduction loss for the discrete strategy becomes

$$\frac{P_{COND}}{P_o} = x \frac{R_{sw}}{NR} . \qquad \text{(V-14)}$$

The conduction loss for the progressively-phase-displaced PWM strategy is next considered. In this case, each switch has a duty cycle d = x; therefore, the switch average and rms currents are given by:

$$i_{avg} = x \frac{V_o}{NR} \text{ and}$$

$$i_{rms} = \sqrt{x} \frac{V_o}{NR} . \qquad \text{(V-15)}$$

The total conduction loss for this case is therefore also given by (V-13), assuming constant-voltage-drop switches, or by (V-14), assuming resistive switches.

In the case of discrete/PWM control, a number of the switches given by int {xN} (the integer part of xN) are continuously on, while one operates with PWM having the duty cycle d = xN - int {xN}. The remaining switches are continously off. The total conduction loss assuming constant-voltage-drop switches is:

$$P_{COND} = \text{int } \{xN\} \left(\frac{V_o}{NR}\right)(V_{sw})$$

$$+ \left[(xN - \text{int } \{xN\}) \frac{V_o}{NR}\right](V_{sw}) . \qquad \text{(V-16)}$$

If resistive switches are assumed,

$$P_{COND} = \text{int } \{xN\} \left(\frac{V_o}{NR}\right)^2 (R_{sw})$$

$$+ \left[(\sqrt{xN - \text{int } \{xN\}}) \frac{V_o}{NR}\right]^2 (R_{sw}) . \qquad \text{(V-17)}$$

As before, (V-16) and (V-17) reduce to (V-13) and (V-14), respectively. There is therefore no difference among these switching strategies in terms of conduction losses.

The expected switching losses are next compared. In each case, the peak

switch current is V_o/NR. The energy lost per switching event (E_{sw}) is therefore considered the same in each case. The steady-state switching loss with the discrete strategy is zero. For the progressively-phase-displaced PWM strategy, the total switching loss is

$$P_{sw} = (2N)(E_{sw})\left(\frac{\omega_s}{2\pi}\right). \qquad \text{(V-18)}$$

(Equal turn-on and turn-off losses are assumed.) In the case of the discrete-PWM strategy, only one switch is actively switching in the steady-state, so for this case

$$P_{sw} = (2)(E_{sw})\left(\frac{\omega_s}{2\pi}\right). \qquad \text{(V-19)}$$

Table V-1 summarizes this comparison of the three proposed switching strategies. The discrete strategy provides the lowest loss and ripple possible; but, due to its high output impedance and discretized output voltage, it is not considered further. The progressively-phase-displaced PWM strategy provides one-Nth the ripple and N-times the switching losses of the discrete/PWM strategy for a given switching frequency. Therefore, neither approach has an advantage (the discrete/PWM strategy could merely be switched at $N\omega_s$ to become equivalent to the progressively-phase-displaced PWM approach). The discrete/PWM strategy was implemented experimentally because its controller is simpler, and it readily works around a faulty ballast section.

Table V-1. Comparison of Three Proposed Switching Strategies

	Discrete Strategy	Prog.-Phase-Disp PWM Strategy	Discrete/PWM Strategy
Output Ripple-Dominant Frequency	----	$N\omega_s$	ω_s
Output Ripple-Magnitude Dom. Component	0	$\frac{2V_o}{\pi N^2 R\omega_s C_o} V_{peak}$	$\frac{2V_o}{\pi NR\omega_s C_o} V_{peak}$
Normalized Conduction Loss $\frac{P_{COND}}{P_o}$	$x \frac{V_{sw}}{V_o}$ or $x \frac{R_{sw}}{NR}$	same	same
Switching Loss P_{sw}	0	$2N E_{sw} f_s$	$2 E_{sw} f_s$

Shunt Regulator Controller

A simplified diagram of the proposed discrete/PWM switch controller is shown in Fig. V-3. The shunt-regulator output voltage v_o is compared with the reference voltage v_{REF}, and then processed by a proportional-integral compensator to form the control voltage v_c. The switch existence functions $s_o \ldots s_{N+M-1}$ are generated by comparison of v_c with the voltages $v_{to} \ldots v_{t(N+M-1)}$ appearing on the resistor chain. Because the resistor chain is fed from the constant-current source I, there is a progressive offset of IR in these voltages; therefore, increasing control voltage will cause progressive turn-on of the switches. This is the discrete portion of the control action.

The PWM portion of the control action is provided by the sawtooth reference generator composed of the MOSFET switch, capacitor C, SR flip-flop and comparators. The resulting waveforms are shown in Fig. V-4. The period of the sawtooth reference is given by

$$T_s = \frac{I'}{I} RC \ ; \qquad \text{(V-20)}$$

its amplitude is given by

$$V_{SAW} = I'R \ . \qquad \text{(V-21)}$$

The control voltage v_c is also shown in Fig. V-4, using a solid line for a steady-state condition, and a broken line for a large transient. The switch existence functions resulting from the steady-state waveforms of Fig. V-4 would be $s_o=1$, $s_2 \ldots s_{N+M-1}=0$ and $s_1=d(t)$; that is, s_o is on, s_1 is pulse-width modulated and the others are off. Examination of the assumed rapid slewing of v_c (the broken line) shows that this controller is capable of rapidly responding to a large transient event, such as a large load step-change. In this case, it is possible for <u>all</u> switches to operate within one switching period, even though this would not occur in the steady-state.

Fig. V-4 is drawn assuming that $I' \cong I$, thus making the successive waveforms nearly continguous. This would normally be desirable in practice because

it eliminates both a possible deadzone in the control action (if I' < I) and the possibility of the application of PWM to two switches simultaneously (if I' > I). (The latter case would correspond to a region of doubled incremental gain in the control characteristic.) The I'/I ratio was made adjustable in the experimental controller so that the deadzone could be trimmed out.

The discrete/PWM controller of Fig. V-4 is shown equiped for N + M switches, of which M are redundant. Replacement of a failed switch is automatic: for example, if s_{N-1} were to fail open-circuited, v_o would rise resulting in an increase in v_c and turn-on of s_N. Failure of a switch in a short-circuit mode would be handled in a similar manner. The deadzone in the control characteristic resulting from failure of a switch could be tolerated, or one of the optional switches $k_o \ldots k_{N+M-2}$ could be closed to remove the deadzone by shorting the appropriate resistor in the chain. It would also be possible to use a digital logic array to redirect the control signal from a faulty switch to one of the spares. If the total number of sections N + M becomes large, this may be preferable, as it would ease the analog design problems associated with a very long string of resistors. (The bias currents and input impedances of the comparators disturb the voltages $v_{to} \ldots v_{t(N+M-1)}$. Also, the magnitudes of these voltages must decrease with increasing length of the resistor chain.) The circuit of Fig. V-3 is conceptually simple, however, and automatically and rapidly applies discrete or PWM control to a ballast section as needed.

The schematic diagram of the controller as implemented experimentally is shown in Fig. V-5. This controller can handle four switches as designed, although only two were needed for the rated power of 2.5 kW. Three switches were actually used in the experimental hardware, so that change-over to a spare switch could be demonstrated. The switching frequency of the PWM switch is approximately 20 kHz. This value was chosen somewhat arbitrarily, although it is low due to the need to keep switching losses low. The two limiting factors were:

1) the use of BJT switches (the only switches available with T_J (max) = 200°C) and

2) the inductance in the cabling connecting the ballast resistors to their switches (these resistors will certainly need to be remotely located).

Fig. V-6 illustrates the base-drive circuitry used in a shunt section. The main

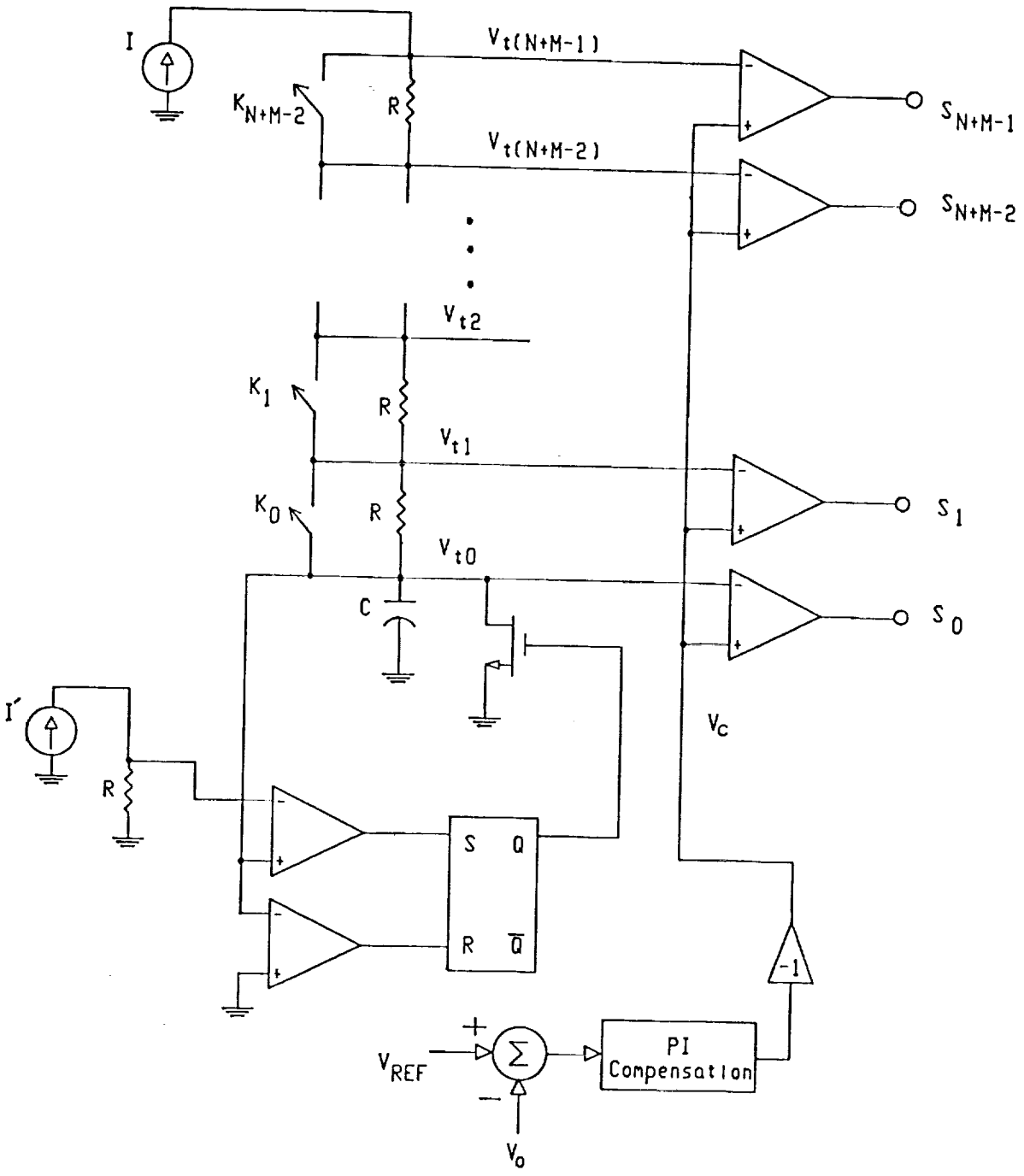


Fig. V-3. Simplified diagrams of discrete/PWM switch controller.

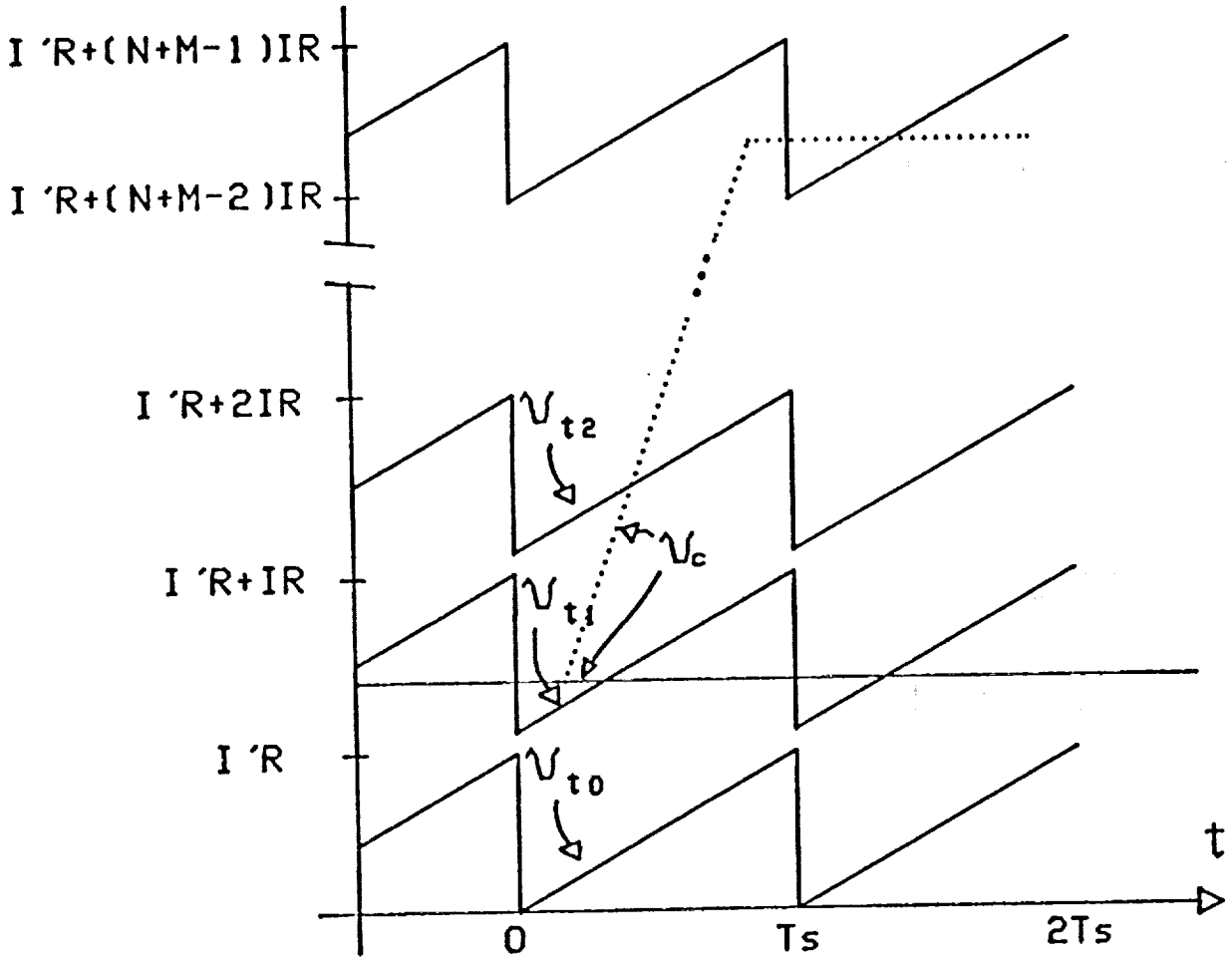


Fig. V-4. Waveforms appearing in the discrete/PWM controller of Fig. V-3.

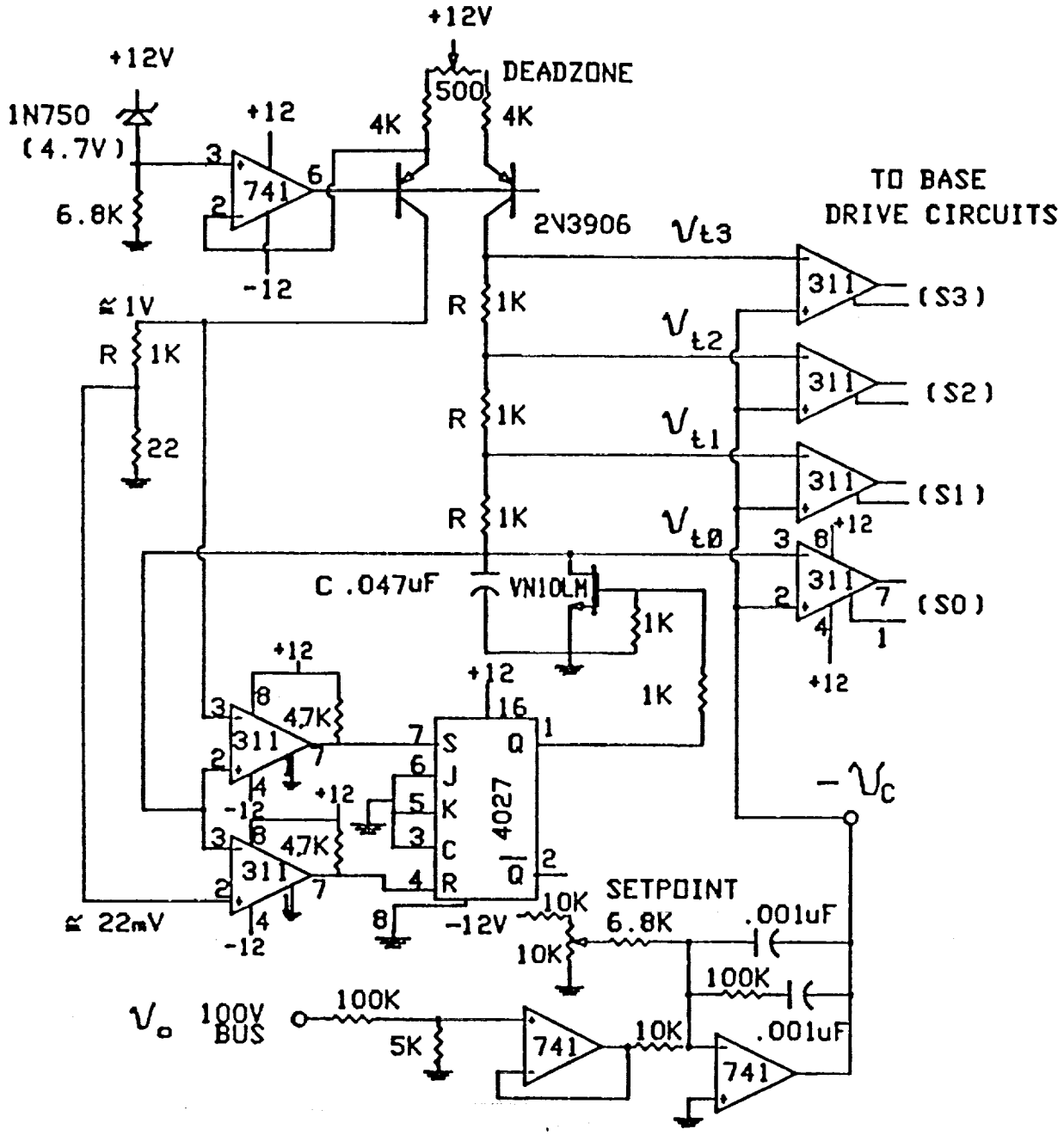


Fig. V-5. Discrete/PWM controller for shunt regulator.

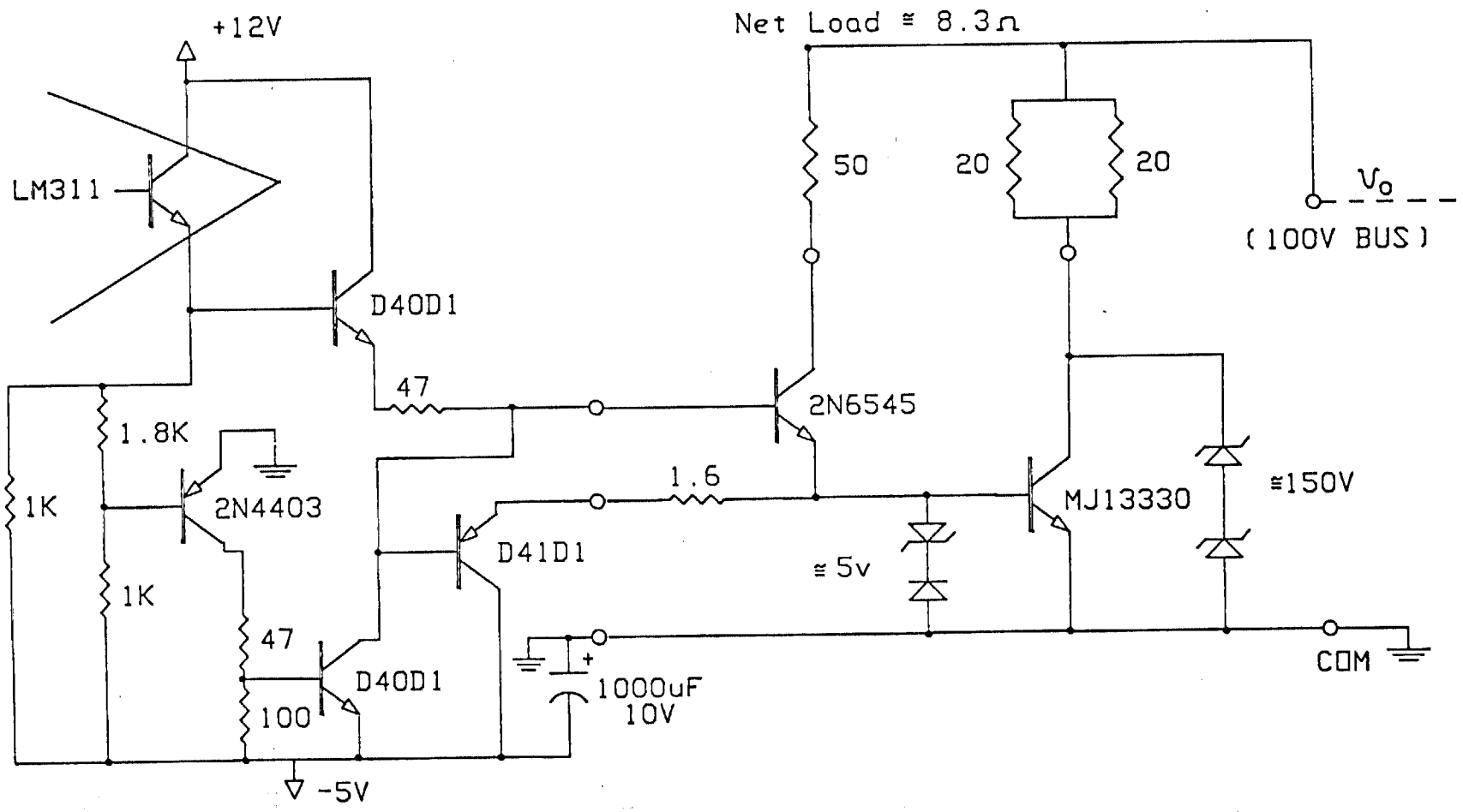


Fig. V-6. Base-drive and switching circuit for one shunt section.

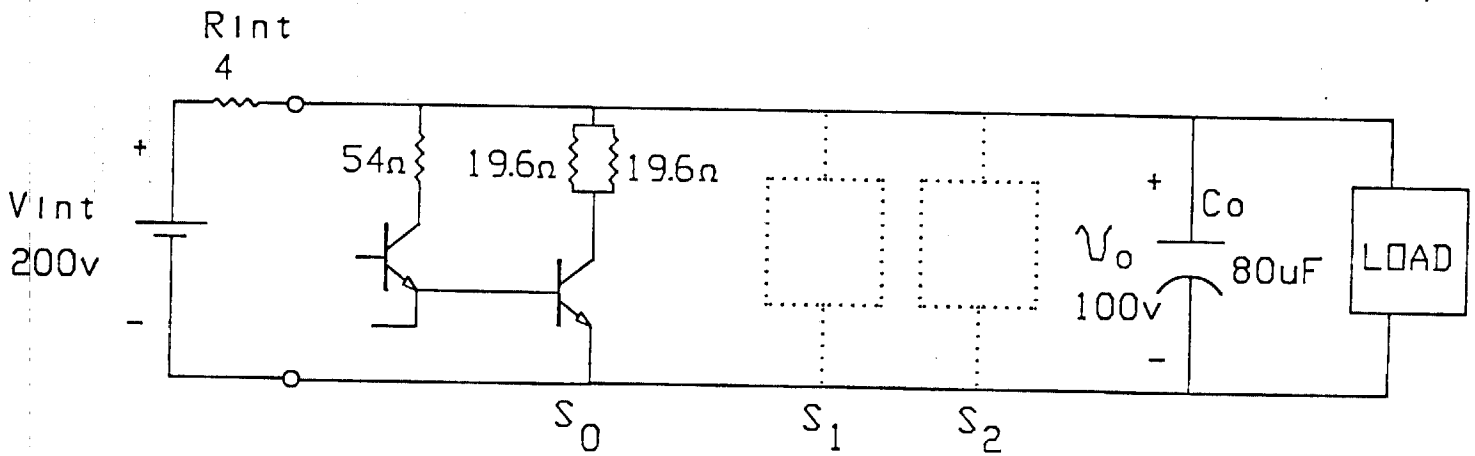


Fig. V-7. Power circuit of 2.5 kW shunt regulator.

switch is the MJ13330, which handles about 10A at 100V (resistive). As mentioned previously, significant cabling inductance is anticipated; a zener voltage clamp was found desirable. Proportional base drive is easily implemented by proportioning the 2N6545 collector resistor appropriately. A 5:1 I_C/I_B ratio was used for the MJ13330 as a compromise between lowered conduction loss and the avoidance of deep saturation with increased turn-off loss. Reverse base current is provided for both the driver and switching transistors. The 1.6 Ω resistor limits the reverse base current applied to the MJ13330 and damps a resonance involving the cabling inductance and the base-emitter capacitance. The 5V zener clamp at this base-emitter junction prevents reverse-breakdown of the junction due to this inductance.

Fig. V-7 shows the power circuit of the complete shunt regulator. Three shunt sections were built, one of which is redundant. The thermoelectric converter was simulated using 200V in series with 4Ω. All power resistors were remotely located (in water buckets) using cables approximately three feet long. The MJ13330 and its 2N6545 driver were mounted on an aluminum plate with heaters so that 120°C operation could be evaluated.

Steady-State Performance

The steady-state performance of the shunt regulator was verified in two areas: 1) the controller operation, including automatic bypass of a failed shunt section, was verified and 2) the base-drive waveforms and switching loss of a shunt section were recorded. Because an integrating controller was used, the steady-state accuracy of the output voltage was limited only by the accuracy with which it was sensed.

Figs. V-8 and V-9 document the operation of the controller of Fig. V-5. The sawtooth waveforms appearing in these figures are v_{t3} . . . v_{to}, from top to bottom. The approximately horizontal line is the control voltage v_c. All waveforms have the same scale factor and offset (0.5V/div, baseline at bottom). The regulator is shunting 5A at 100V, which requires only one section operating at approximately 50 percent duty cycle. Unlike the conceptual diagram of Fig. V-3, the shunt

sections are activated in descending order in the actual circuit of Fig. V-5. This means that the shunt current increases as v_c decreases. As implied by Figs. V-8 and V-9, switches s_3 and s_2 were unavailable during this experiment. In Fig. V-8, the first available switch was s_1. Fig. V-9 shows the result of disabling s_1 (by open-circuiting it): v_c decreases causing the controller to automatically pick-up s_o. The switching noise apparent in Figs. V-8 and V-9 did not seem to affect the proper operation of the controller. It would be reduced by a better circuit layout technique (perf-board and point-to-point wiring was used).

Figs. V-10 to V-13 display the switching waveforms found in a shunt section operating at about 50 percent duty cycle on a 40°C baseplate. The base and collector currents (i_B and i_C), and collector-emitter voltage (v_{CE}) of the MJ13330 are shown in Fig. V-10. It may be noted that the peak collector current is constant (at 10A in this case) with regard to the duty cycle. This allows easy implementation of proportional base drive: a forced beta of 5 was used here. Figs. V-11 and V-12 show details of turn-on and turn-off, respectively. Fig. V-13 shows the i_c-v_{CE} product waveform at 100 W/div. Using the waveform measurement capabilities of the oscilloscope, the switching and conduction loss data of Table V-2 were determined. It should be noted that the current and voltage waveforms in Fig. V-13 have been event-averaged to reduce their noise levels. The i-v product waveform displayed in this figure is the product of these averaged waveforms. The area under this product waveform was measured. The total loss was 973 μJ (20.1 W at the 20.7 kHz switching frequency). This loss was subdivided into turn-on, turn-off and conduction-interval components using manual positioning of the oscilloscope measurement cursors.

Fig. V-14 shows the switching waveforms obtained while operating on a 120°C baseplate. These were also processed by event-averaging; the results are displayed in Fig. V-15 with the resulting product waveform. Switching and conduction loss data at 120°C are also listed in Table V-2. The transistor junction temperature was estimated in each case based on the measured total power dissipation, $\theta_{JC} = 1 c^o/w$ and $\theta_{cs} \cong 0.5 c^o/w$.

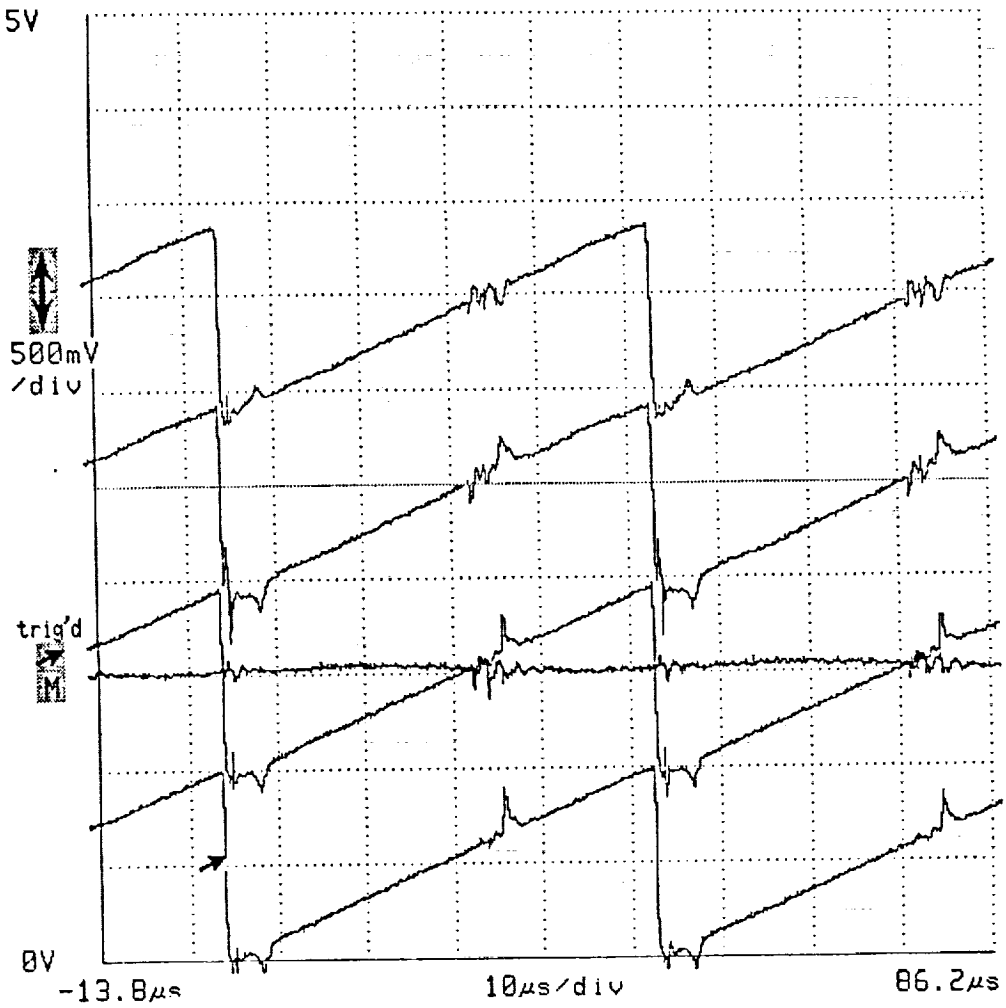


Fig. V-8. Sawtooth reference voltages v_{t3} . . . v_{to} (top to bottom) and control voltage vc (all at 0.5 V/div). PWM applied to s1.

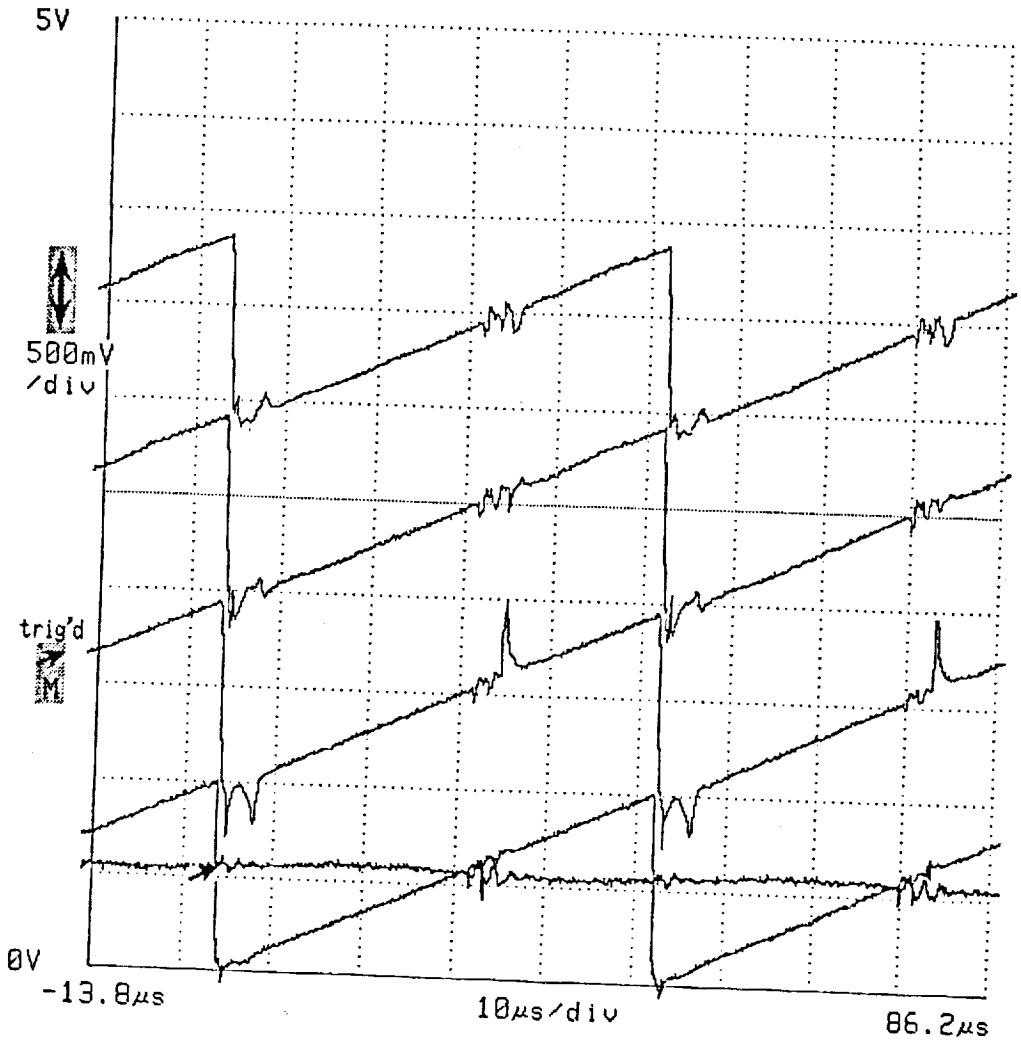


Fig. V-9. Sawtooth reference voltages v_{t3} . . . v_{to} (top to bottom) and control voltage v_c (all at 0.5 V/div). PWM applied to s_o.

Table V-2

Losses in MJ13330 Shunt Switch

Item	Baseplate Temperature 40°C	120°C
Turn-On Loss	3.7 W	12.0 W
Turn-Off Loss	10.7 W	20.4 W
Conduction Loss	5.8 W	7.1 W
Total Loss	20.1 W	39.4 W
Junction Temperature*	70°C	179°C
Peak Current	10 A	same
Peak Voltage	100 V	same
Frequency	20.7 kHz	same

*Estimated based on θ_{JC} = 1C°/w and θ_{cs} = 0.5C°/w.

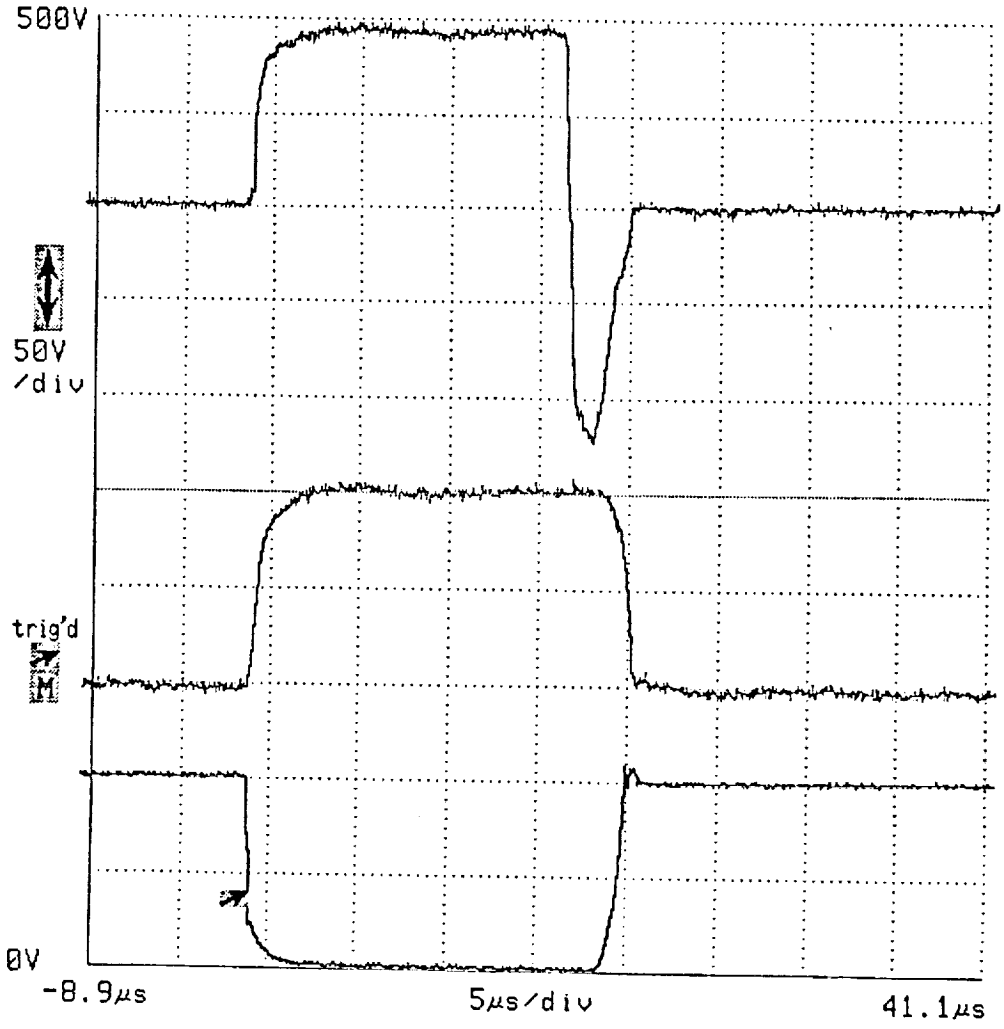


Fig. V-10. Switching waveforms from MJ 13330 at 40°C. Top: i_B at 1 A/div. Middle: i_c at 5 A/div. Bottom: v_{CE} at 50 v/div. Timebase: 5 μ s/div.

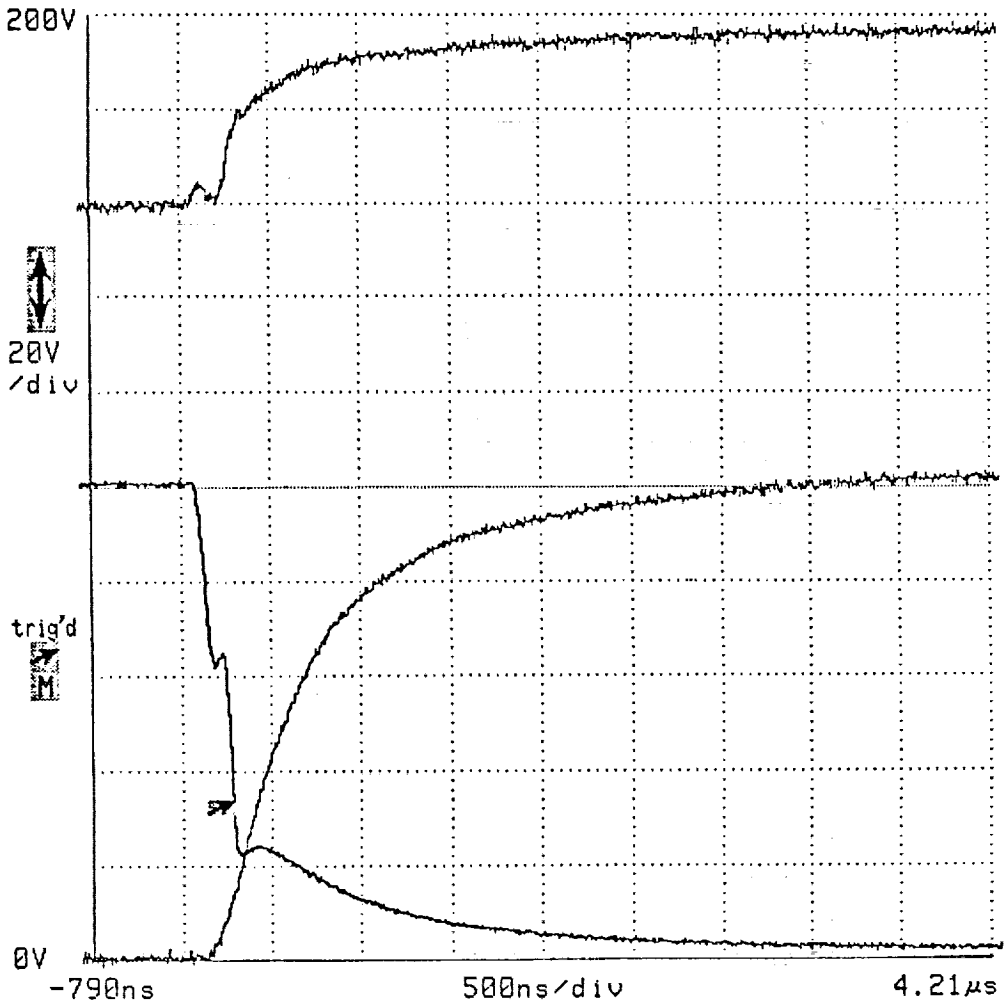


Fig. V-11. Detail of MJ13330 turn on. Top: i_B at 1 A/div. Bottom: i_c at 2 A/div. and v_{CE} at 20 v/div. Timebase: 500 ns/div.

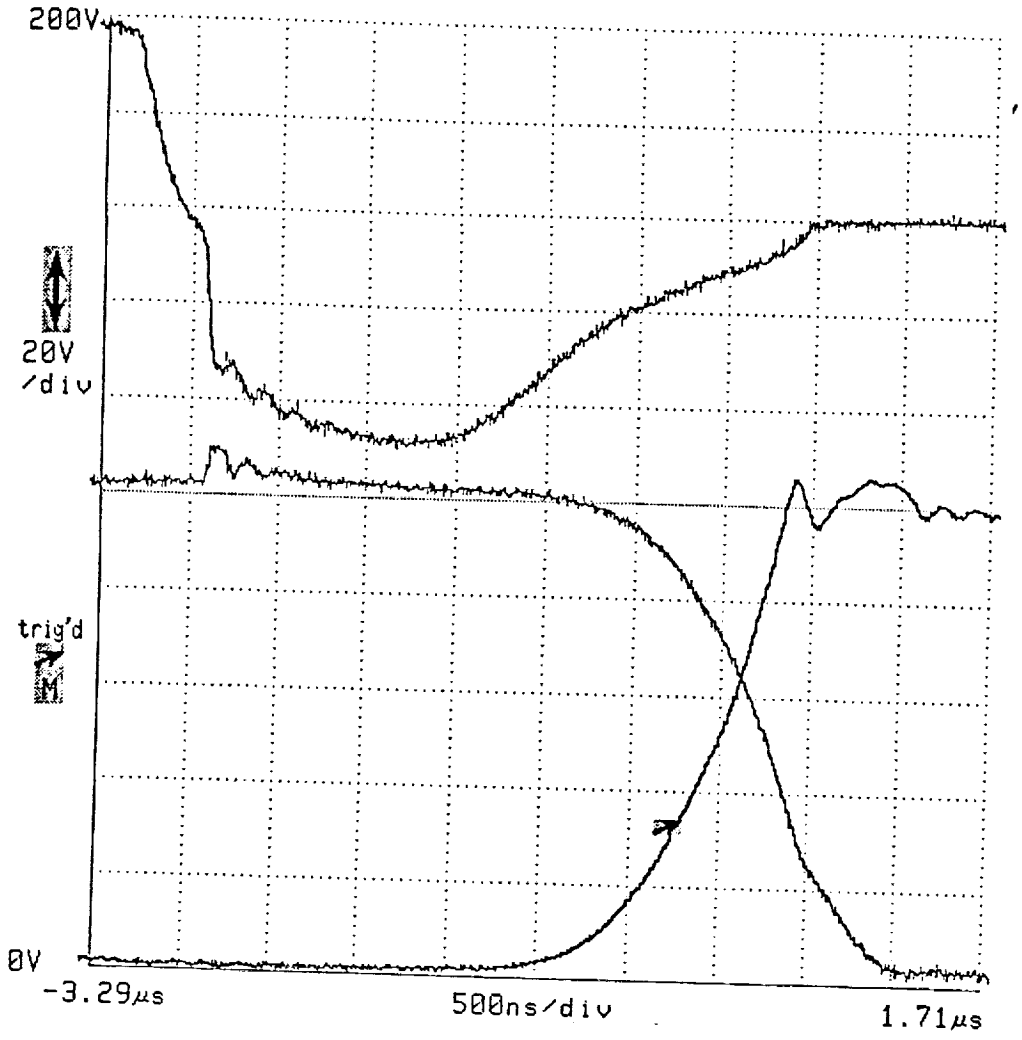


Fig. V-12. Detail of MJ13330 turn off. Top: i_B at 1 A/div. Bottom: i_c at 2 A/div. and v_{CE} at 20 V/div. Timebase: 500 ns/div.

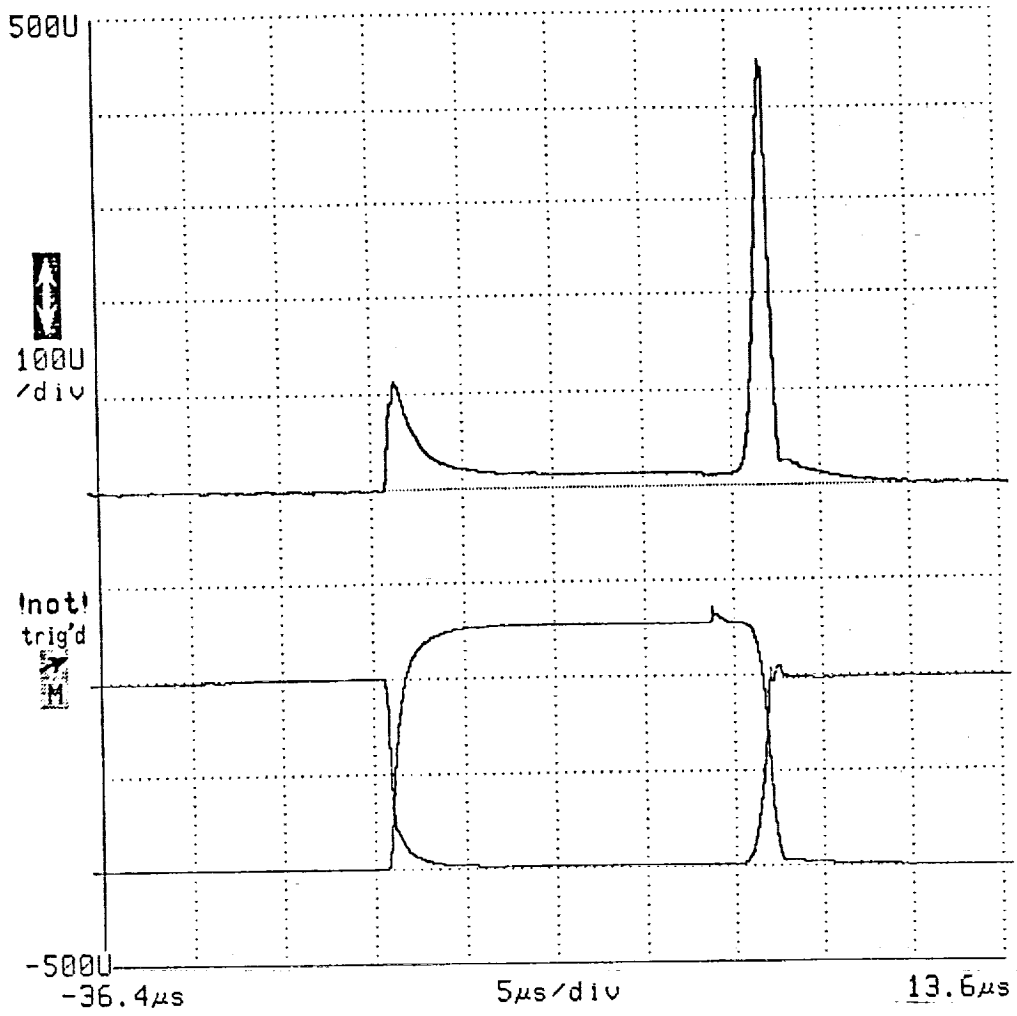


Fig. V-13. Switching and conduction losses of MJ13330 at 40°C.
Top: $i_c(t)$ $v_{CE}(t)$ at 100 w/div. Bottom: i_c at 4 A/div. and v_{CE} at 50 V/div.

C-2

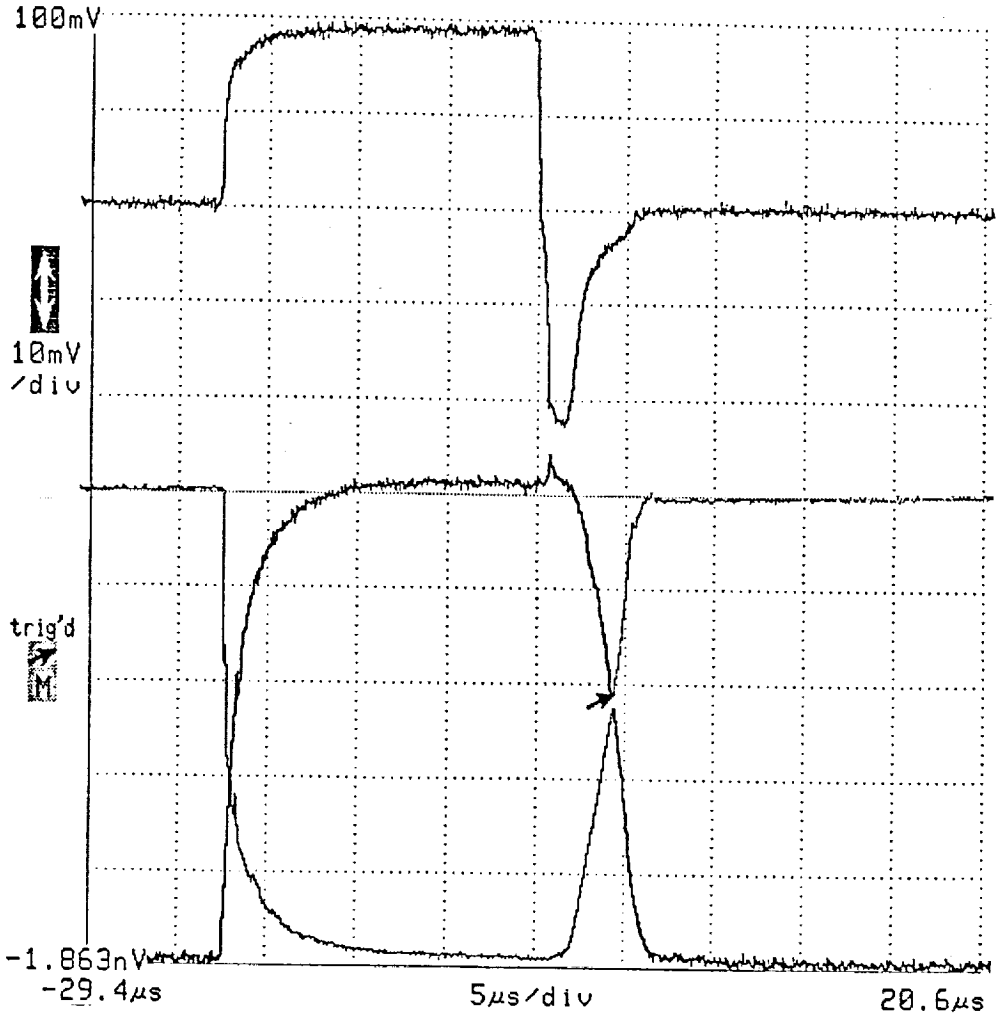


Fig. V-14. Switching waveforms from MJ13330 at 120°C.
Top: i_B at 1 A/div. Bottom i_c at 2 A/div. and v_{CE} at 20 V/div.
Timebase 5μs/div.

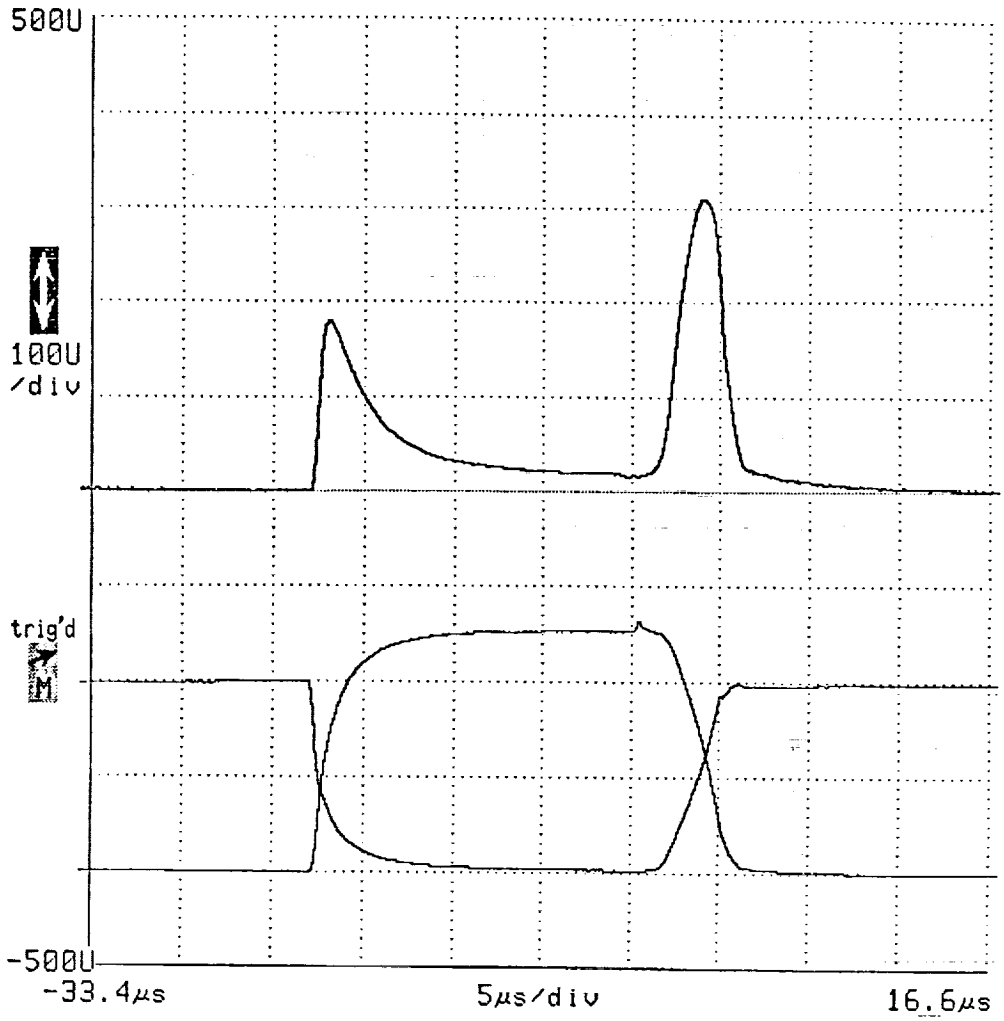


Fig. V-15. Switching and conduction losses of MJ13330 at 120°C. Top: $i_c(t)$ v_{CE} (t) at 100 W/div. Bottom: i_c at 4 A/div. and v_{CE} at 50 V/div.

Transient Modeling of the Shunt Regulator

The application of the proposed TEC-shunt regulator will require a useful transient modeling procedure. The switched nature of the shunt regulator suggests the discrete modeling technique summarized in [6], although the much simpler state-space averaging of [1] should be used instead, if it is applicable.

State-space averaging is justified by assuming that all of the state variables have only a first-order time variation over a switching cycle. This permits the replacement of a succession of switched circuits with a single "equivalent" averaged circuit. The equivalent procedure in state-space notation is the replacement of a succession of A and B coefficient matrices with their time-weighted averages. The result is a time-invariant system, though it is nonlinear due to the fact that the time-durations of the individual equivalent circuits are normally control inputs. This nonlinear time-invariant system can then be conveniently simulated on a general-purpose simulation program such as SPICE, or it can be linearized to find a simpler incremental model. The first step in the application of state-space averaging to the proposed discrete/PWM shunt regulator should be a check of its validity for realistic component values.

The condition of validity for state-space averaging is that the time constant associated with each switched circuit must be much greater than the duration of that equivalent circuit [1]. In the discrete/PWM regulator, there is one state variable in the switched portion of the circuit (v_o). The time constant associated with this circuit varies according to the number of switches closed (see Fig. V-1), but it is restricted by

$$\tau \leq R_{int}\, c_o \ . \qquad \text{(V-22)}$$

If a maximum-power-transfer design is used ($R = R_{int}$), then the output ripple requirement imposes the limit on C_o(from V-11):

$$R_{int}\, C_o = \frac{2}{\pi\, N\, \omega_s \left|\frac{V_R}{V_o}\right|} \ . \qquad \text{(V-23)}$$

Combining (V-22) and (V-23):

$$\tau \leq \frac{1}{\pi^2 N \left|\frac{V_R}{V_o}\right|} T_s \ . \qquad \text{(V-24)}$$

Substituting values of peak output ripple (V_R) ranging from 0.01 V_o to 0.1 V_o, and numbers of sections (N) from 2 to 8, gives the range $\tau \leq 0.13\ T_s$ to $5.1\ T_s$. This suggests that practical design values of C_o might not meet the criterion for state-space averaging.

State-space averaging is, however, still justified for both large-and small-signal modeling of this regulator. The justification is that even though the time constants may be small, they change little over a switching cycle, allowing their average value to be used in an averaged equivalent circuit. To demonstrate this, an exact solution for the natural response of Fig. V-1 over one switching cycle will be computed and compared with that of the averaged model. The comparison will be made for near-steady-state conditions, and also for the largest transient possible.

Incremental signal levels are first considered. With the discrete/PWM control method, only one switch changes state over a switching cycle in the near-steady-state. The two resulting time constant are

$$\tau_1 = R_{int}\, C_o \quad \text{and}$$

$$\tau_2 = k\, \tau_1 = (R_{int} \,\|\, N\, R_{int})\, C_o \ . \qquad \text{(V-25)}$$

In (V-25), the load has been assumed to contain infinite incremental resistance and the regulator switches operating such that the largest change possible in τ is observed. For a change of condition of one shunt switch, the ratio of τ_2 to τ_1 is:

$$k = \frac{\tau_2}{\tau_1} = \frac{N}{N+1} \ . \qquad \text{(V-26)}$$

With a certain duty cycle d, the natural response of Fig. V-1 over one switching cycle would be found as follows:

$$\dot{v}_o = -\tau_1^{-1}\, v_o \ , \ 0 \leq t \leq dT_s$$

$$\dot{v}_o = -\tau_2^{-1} v_o \quad , \quad dT_s \le t \le T_s$$

$$v_o(T_s) = e^{-\frac{1-d}{\tau_2} T_s} e^{-\frac{d}{\tau_1} T_s} v_o(0) \quad \text{or}$$

$$v_o(T_s) = e^{-\frac{T_s}{\tau_{eq}}} v_o(0) \quad \text{where}$$

$$\tau_{eq} \equiv \left(\frac{1-d}{\tau_2} + \frac{d}{\tau_1} \right)^{-1} . \qquad \text{(V-27)}$$

The equivalent time constant of (V-27) is that required of an unswitched equivalent circuit to obtain the same natural response at the end of a switching period as the actual circuit. The state-space-averaged system would be

$$\langle \dot{v}_o \rangle = \frac{-1}{(1-d)\tau_2 + d\,\tau_1} \langle v_o \rangle \, , \; 0 \le t \le T_s$$

with the solution

$$\langle v_o(T_s) \rangle = e^{-\frac{T_s}{\tau_{avg}}} \langle v_o(0) \rangle \quad \text{where}$$

$$\tau_{avg} \equiv (1-d)\,\tau_2 + d\tau_1 \, . \qquad \text{(V-28)}$$

The average time constant of (V-28) is that of the unswitched equivalent circuit produced by state-space averaging. It is apparent that $\tau_{avg} \neq \tau_{eq}$.

The error in the propagation of the state v_o over a switching cycle is estimated by dividing the state-space-averaged result (V-28) by the exact result (V-27), assuming equal initial conditions $v_o(0)$:

$$\frac{\langle v_o(T_s) \rangle}{v_o(T_s)} = e^{\frac{T_s}{\tau_{eq}} - \frac{T_s}{\tau_{avg}}} \cong 1 + \left(\frac{T_s}{\tau_{eq}} - \frac{T_s}{\tau_{avg}} \right) . \qquad \text{(V-29)}$$

The approximation in (V-29) is supplied in the expectation that the two results will be nearly equal. The fractional error term in (V-29) is restated using (V-26), (V-27) and (V-28):

$$\frac{v_o(T_s) - \langle v_o(T_s)\rangle}{v_o(T_s)} = \frac{T_s}{\tau_1}\left[\frac{1-d}{k} + d - \frac{1}{(1-d)k + d}\right]. \qquad \text{(V-30)}$$

Equation (V-30) is differentiated with respect to duty cycle d; the result is equated to zero, producing the expression for the worst-case value of d:

$$d_{wc} = \frac{k - \sqrt{k}}{k - 1}. \qquad \text{(V-31)}$$

Substituting (V-31) back into (V-30) produces the expression for the worst-case fractional error:

$$\left[\frac{v_o(T_s) - \langle v_o(T_s)\rangle}{v_o(T_s)}\right]_{wc} = \frac{T_s}{\tau_1}\,\frac{k^2 - 2k\sqrt{k} + 2\sqrt{k} - 1}{k(k-1)}. \qquad \text{(V-32)}$$

If the output capacitor C_o is sized according to (V-23), then substituting (V-25) into (V-32) gives:

$$\left[\frac{v_o(T_s) - \langle v_o(T_s)\rangle}{v_o(T_s)}\right]_{wc} = \frac{1 - 2\sqrt{k} + 2k\sqrt{k} - k^2}{k(1-k)}\,\pi^2 N\left|\frac{V_R}{V_o}\right|. \qquad \text{(V-33)}$$

As expected, (V-33) shows that the accuracy of state-space-averaging improves with decreasing ripple in the capacitor voltage. Also, an application of L'Hopital's rule shows that

$$\lim_{k \to 1}\left[\frac{v_o(T_s) - \langle v_o(T_s)\rangle}{v_o(T_s)}\right]_{wc} = 0. \qquad \text{(V-34)}$$

This is also expected, because k is the ratio of the two time constants in question, and as k approaches unity, state-space-averaging becomes exact.

Fig. V-16 is a plot of the relative error produced by state-space-averaging over one switching period. In the near-steady-state, Fig. V-16 can be consulted to estimate the percentage error in the output voltage after one switching period. (The value of k is related to the number of switched sections N by (V-26)). A plot similar to Fig. V-16 could also be constructed for the relative error in the apparent time constant of the state-space-averaged model. The conclusion which is drawn from Fig. V-16 is that for reasonable rippple levels in the design, state-space averaging is accurate for even one or two switched sections and small signals.

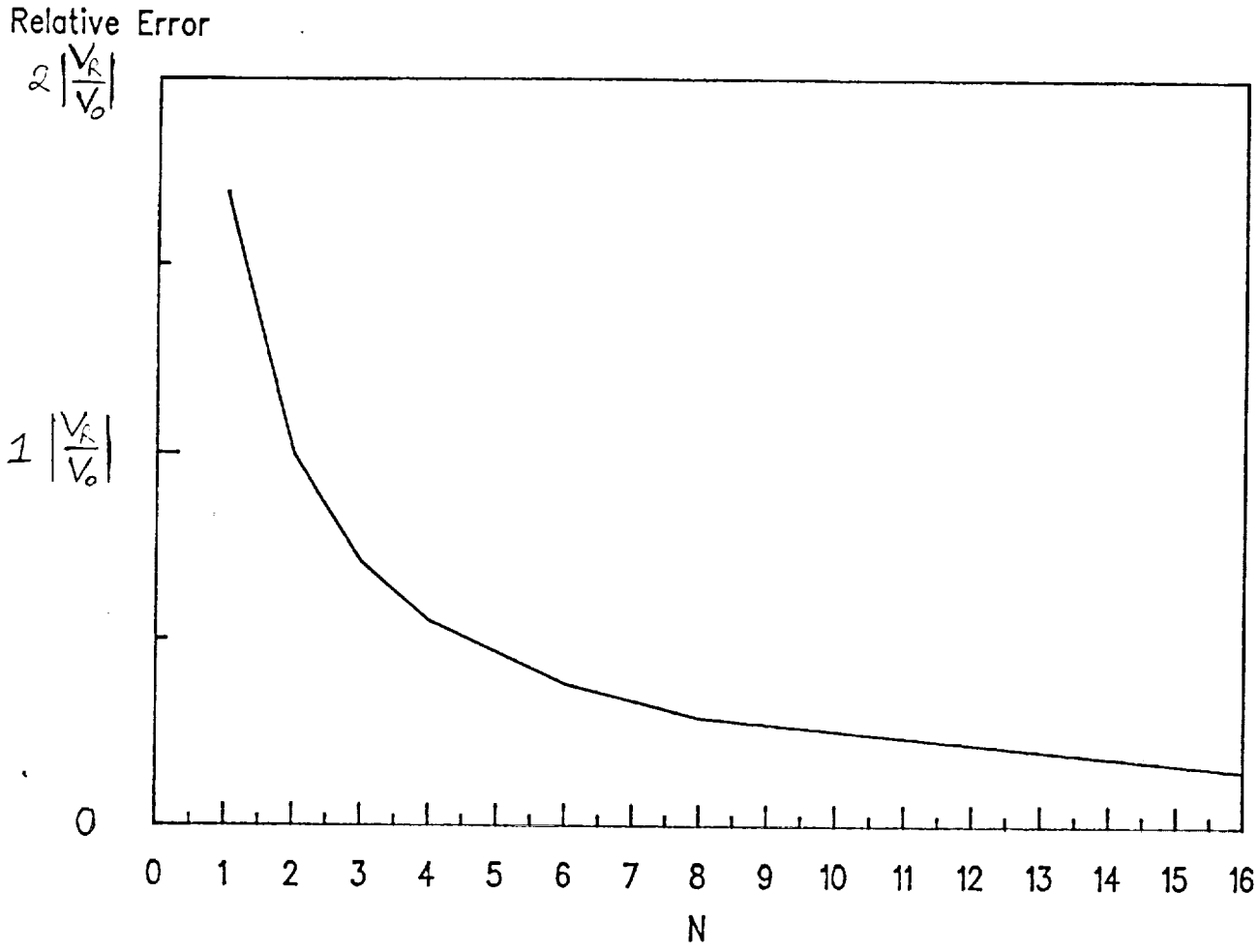


Fig. V-16. Relative error per switching period produced by state-space-averaging versus number of switched sections. Small signal conditions are assumed.

The implications of using a state-space-averaged model for a large-signal transient simulation are next investigated. Equation (V-33) was derived based on an assumed ratio of time constants k and the choice of C_o based on the number of sections N and the ripple requirement $\left|\frac{V_R}{V_o}\right|$. In a large-signal simulation, k is no longer constrained by (V-26); the worst-case value of k would occur if the regulator control voltage v_c would slew so quickly that all switches went from open to closed in one switching period. The value of k under this circumstance would be 0.5. Substituting this value into (V-33) produces the large-signal result

$$\left[\frac{v_o(T_s) - \langle v_o(T_s)\rangle}{v_o(T_s)}\right]_{wc} \leq 1.693\ N\left|\frac{V_R}{V_o}\right|. \qquad \text{(V-35)}$$

Substituting design ripple values from 0.01 V_o to 0.1 V_o and numbers of sections from 2 to 8 into (V-35) produces worst-case one-cycle simulation errors ranging from 0.034 to 1.36. These results represent the departure of the state-space-averaged simulation from the actual result over one switching period, assuming the largest conceivable transient. For low-ripple designs having small N the error is quite low, however, there will be some loss of accuracy with large N and small C_o. The state-space-averaged model is quite useful due to its simplicity and ease of use, and was therefore used in this investigation. The results of this modeling technique are next compared with the experimental performance of the shunt regulator.

Dynamic Performance

The experimental dynamic performance of the shunt regulator is compared with that predicted by a PSpice [7] simulation of the nonlinear state-space-averaged model of the experimental hardware in two areas: 1) the incremental output impedance and 2) the response to a large load current step change. The averaged model is first presented in the form of an equivalent circuit used for PSpice simulation. This is shown in Fig. V-17. The state-space-averaging has taken place in representing three switched shunt resistor sets by the voltage-controlled conductor "GISH". An exact model of the shunt resistor sections would be the discrete model:

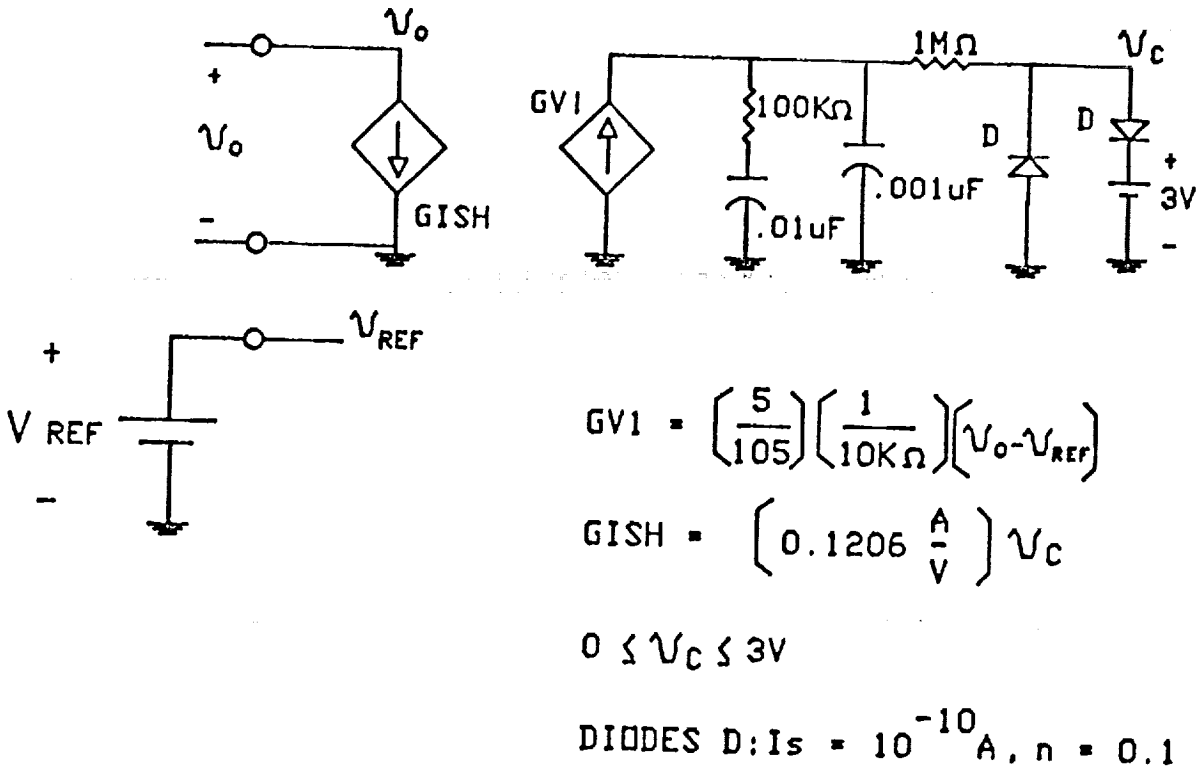


Fig. V-17. Simplified PSpice simulation model of shunt regulator with voltage regulator.

$$y_{SH} = \frac{n(t)}{NR} \ , \ n = 0, 1, 2, 3$$
$$\text{and } N = 3 \ , \ R = 2.78\Omega \ . \qquad \text{(V-36)}$$

This has been replaced in Fig. V-17 by the averaged model:

$$y_{SH} \cong \frac{x(t)}{NR} \ , \ 0 \le x \le 3$$
$$\text{and } N = 3 \ , \ R = 2.78\Omega \qquad \text{(V-37)}$$

Note that the simulation model of Fig. V-17 is nonlinear due to the voltage - controlled conductor. An incremental equivalent circuit could easily be derived; in this work the incremental analysis capability of PSpice was used instead.

The incremental output impedance of the shunt regulator was first computed using PSpice for $R_{int} = 4.5\Omega$ and two different values of C_o: 80μF and 380μF. The 80μF capacitor was composed of four paralleled polypropylene units and assumed ideal. The 380μF capacitor was composed of the 80μF together with six paralleled Sprague 39D electrolytic units. The latter were modeled by a 263μF capacitor in series with 0.124Ω, based on a 10 kHz impedance measurement. The output impedance with C_o = 80μF is shown in Fig. V-18 (magnitude) and Fig. V-19 (phase). Experimental data points are indicated on each figure, showing good agreement. The operating point used was a load current of 1Adc; even though the circuit is nonlinear, the PSpice analysis showed negligible dependance of the output impedance on the operating point. The output impedance with C_o = 380μF is shown in Fig. V-20 (magnitude) and Fig. V-21 (phase). The experimental data points are also indicated on these figures, again showing good agreement. There are two significant discrepancies between the experimental and predicted results: 1) the low-frequency phase measurements at 20 and 40 Hz and 2) the high -frequency phase measurements above 10kHz. The former is believed due to measurement error (inadequate signal level at the low-frequency limit of the measuring equipment). The latter is believed due to incomplete modeling of the ESR characteristics of the output bypass capacitor, because the output impedance

above 10kHz is dominated by this component.

The transient simulation of the model of Fig. V-17 was also verified experimentally. A step application and removal of a 8.3Ω load resistance (approximately half-load) was simulated using PSpice. Two different values of C_o were considered: $C_o = 80\mu F$ and $C_o = 380\mu F$. The same transient was then observed experimentally. Fig. V-22 is a plot produced by PSpice; Fig. V-23 is the corresponding experimental result. Each of these figures displays $v_o - 100$, where v_o is the output voltage (the regulator setting is 100 V). The experimental result, Fig. V-23, displays two traces: the upper is an unprocessed version of $v_o - 100$ at 5 V/div, the lower is an event-averaged version of $v_o - 100$ at 2 V/div. (It can be seen that event averaging reduces the switching noise obscuring the transient.) Figs. V-24 and V-25 display expanded views of the same transient for the simulation and experiment respectively. Good agreement is seen in Figs. V-22 to V-25 for both amplitudes and times of the transient.

The same transient was studied with $C_o = 380\mu F$ (the model of the 380 μF capacitor which includes the ESR previously referred to was used). The PSpice simulation is shown in Fig. V-26; the experimental result is shown in Fig. V-27. The unprocessed experimental waveform is shown at 5 V/div; the event-averaged waveform is shown at 2 V/div as before. Good agreement is again obtained.

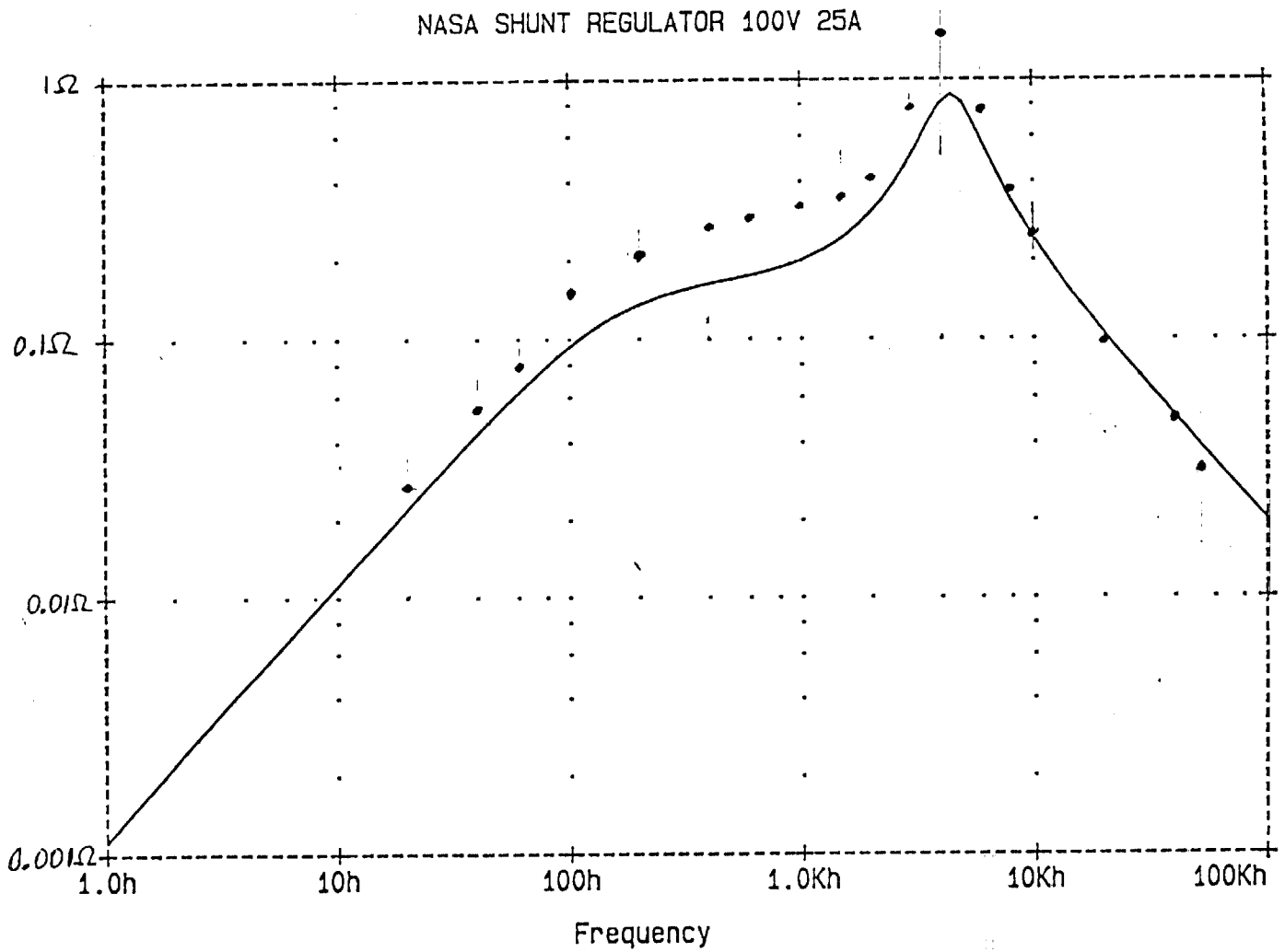


Fig. 18. Magnitude of shunt regulator output impedance, $c_o = 80\mu F$. Experimental data points are indicated.

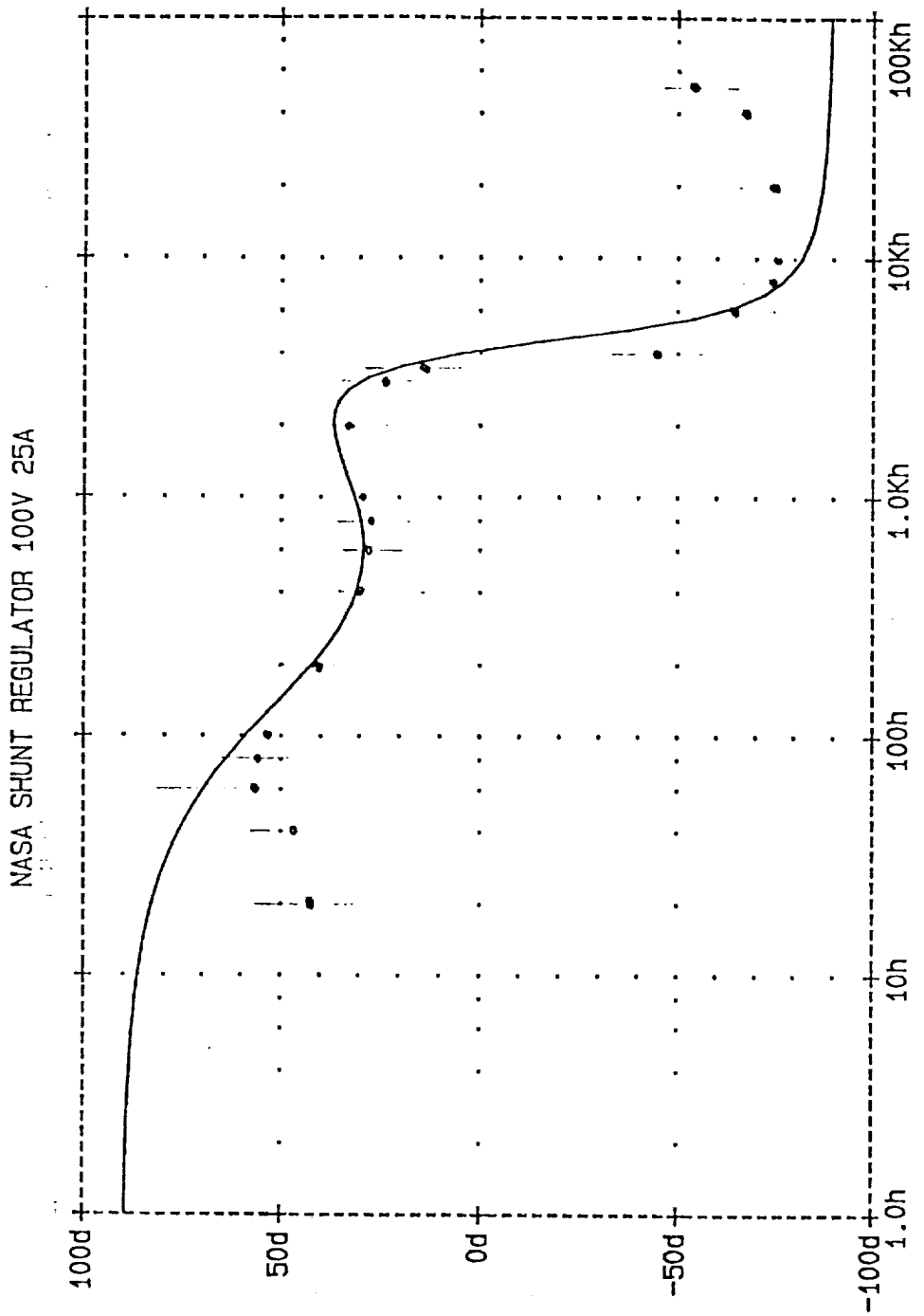


Fig. 19. Phase of shunt regulator output impedance, $c_o = 80\mu F$. Experimental data points are indicated.

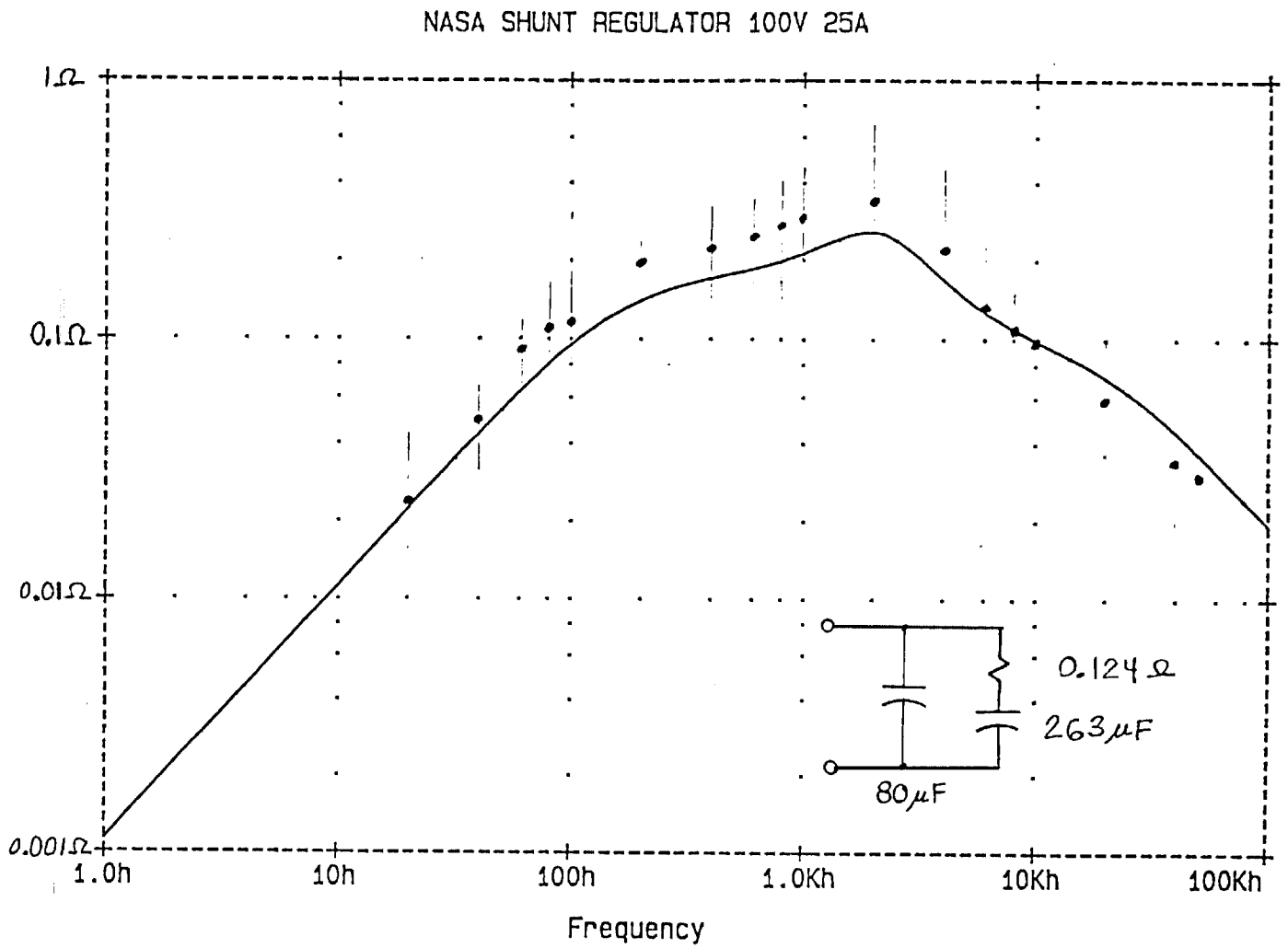


Fig. V-20. Magnitude of shunt regulator output impedance, c_o=380μF (nom.) The capacitor model is indicated. Experimental data points are indicated.

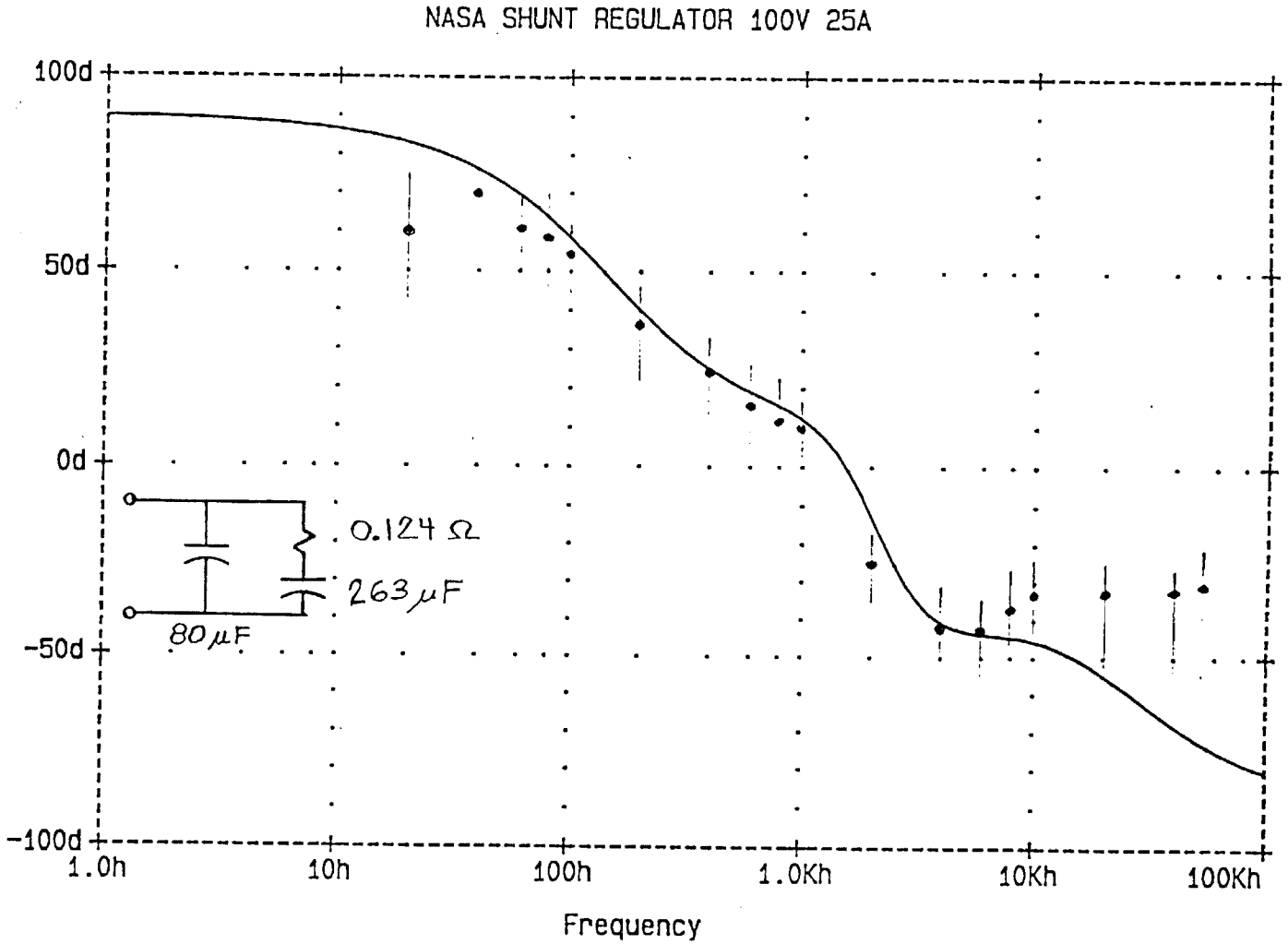


Fig. V-21. Phase of shunt regulator output impedance, $c_o = 380\mu F$ (nom.). The capacitor model is indicated. Experimental data points are indicated.

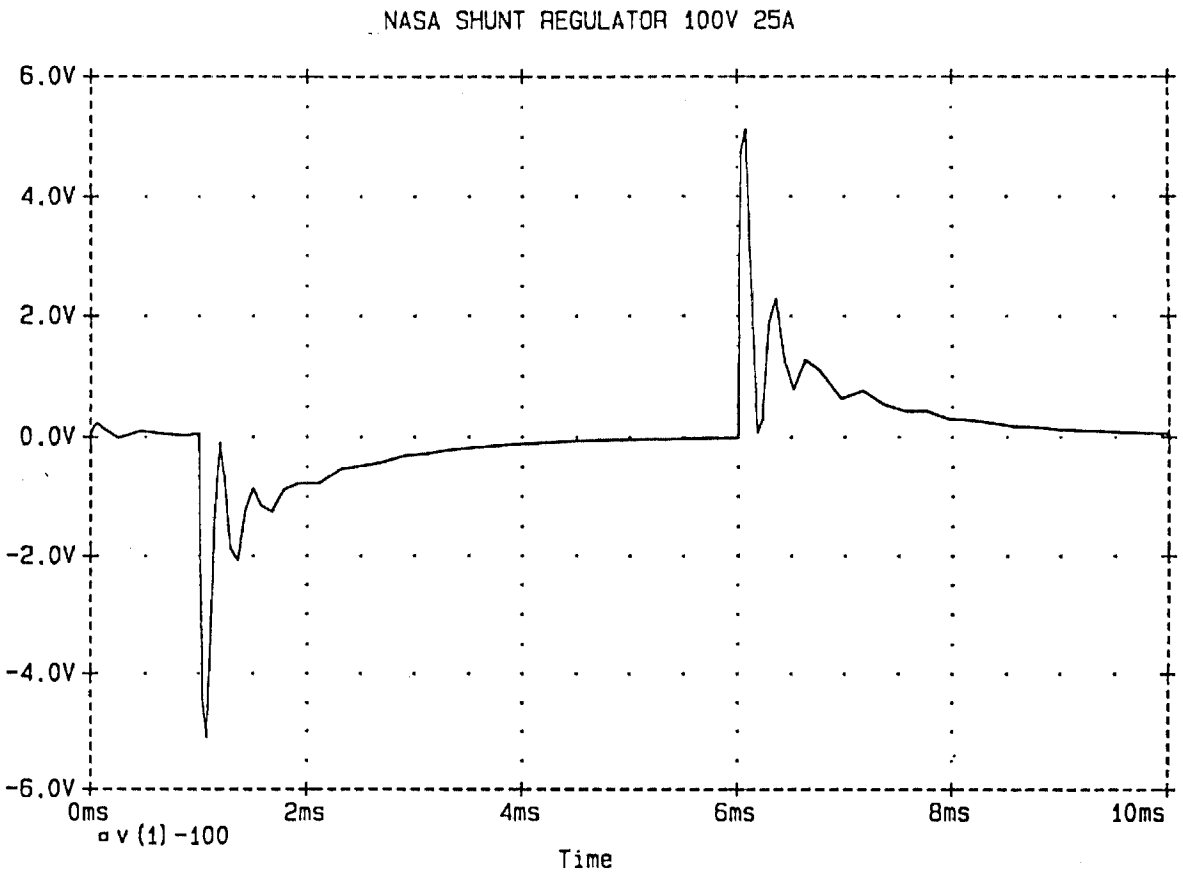


Fig. V-22. PSpice simulation of load step-change with $c_o = 80\mu F$. Shown is $v_o - 100$.

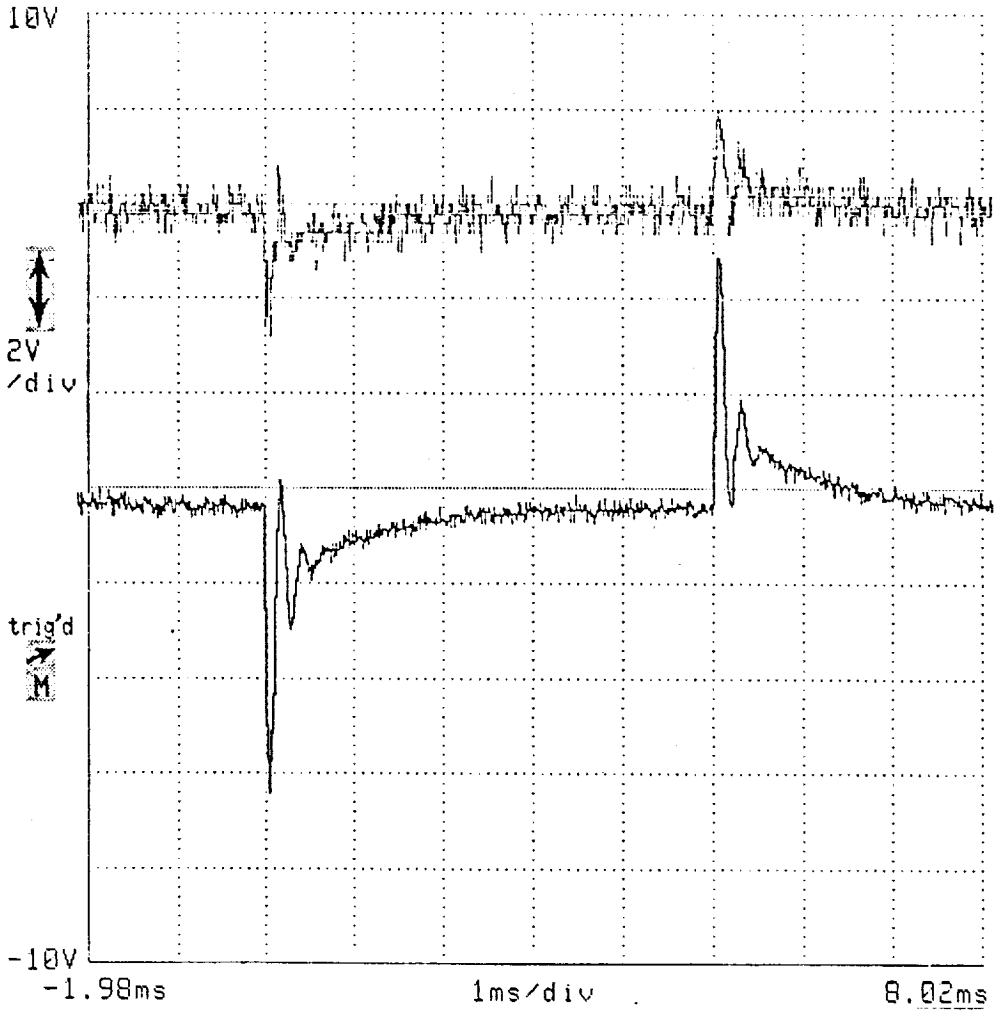


Fig. V-23. Experimental load step-change with c_o = 80μF. Upper: v_o - 100 at 5 V/div (unprocessed). Lower: v_o - 100 at 2 V/div (event-averaged). Timebase: 1 mS/div.

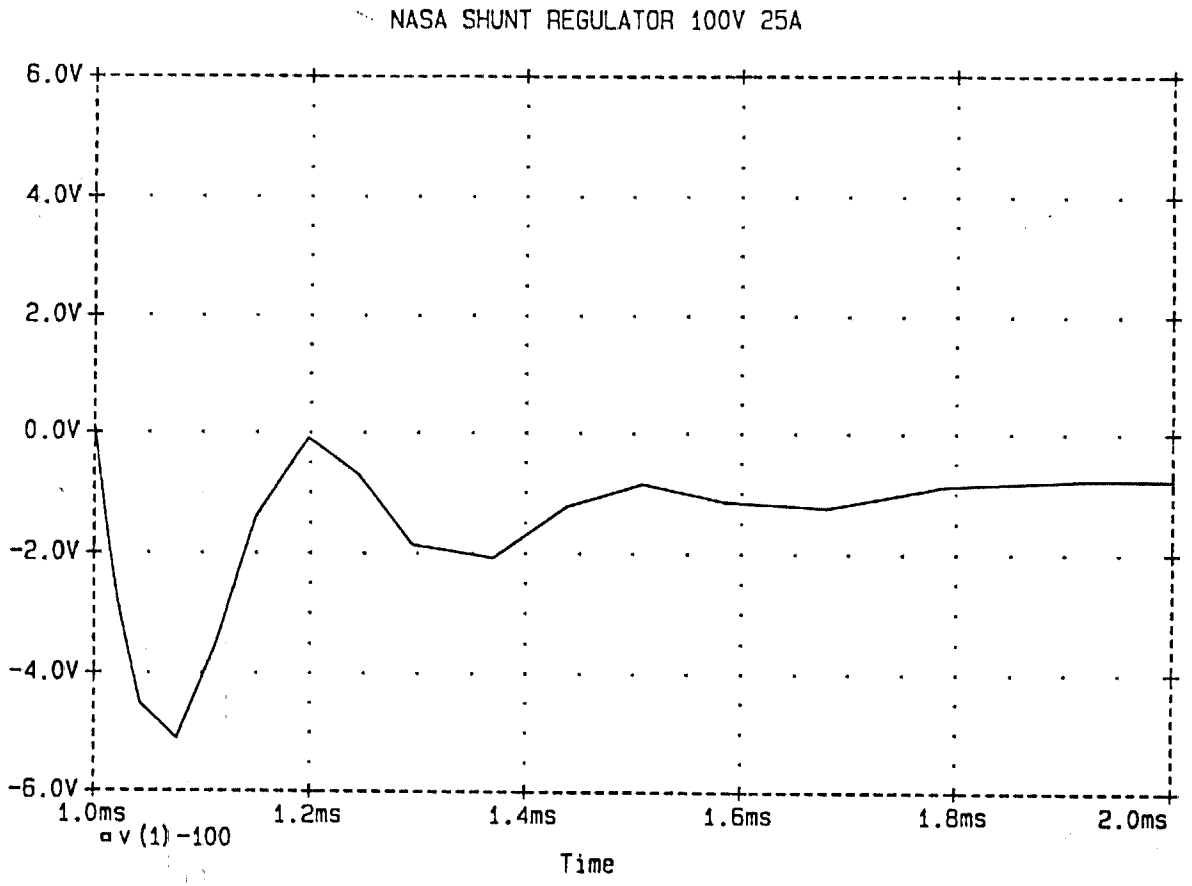


Fig. V-24. Expanded view of Fig. 22.

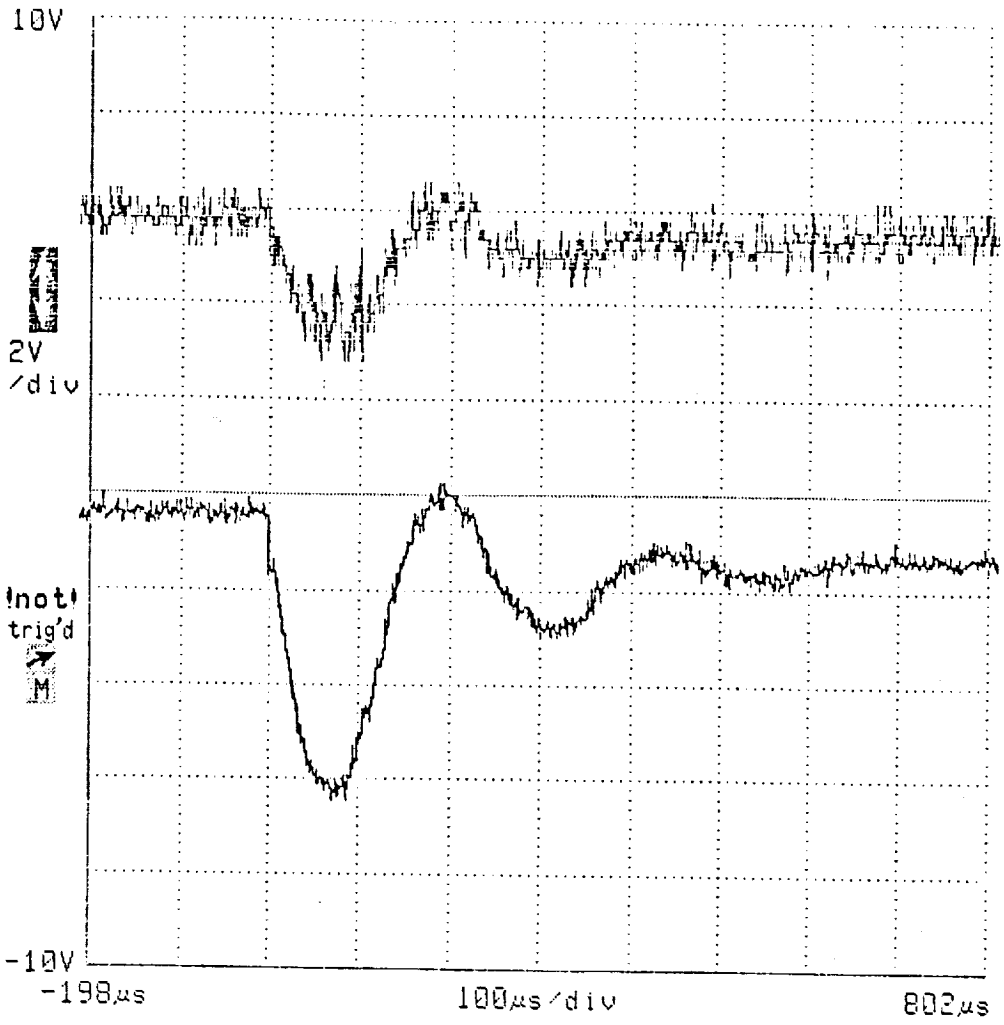


Fig. V-25. Expanded view of Fig. III-23. Timebase: 100µS/div.

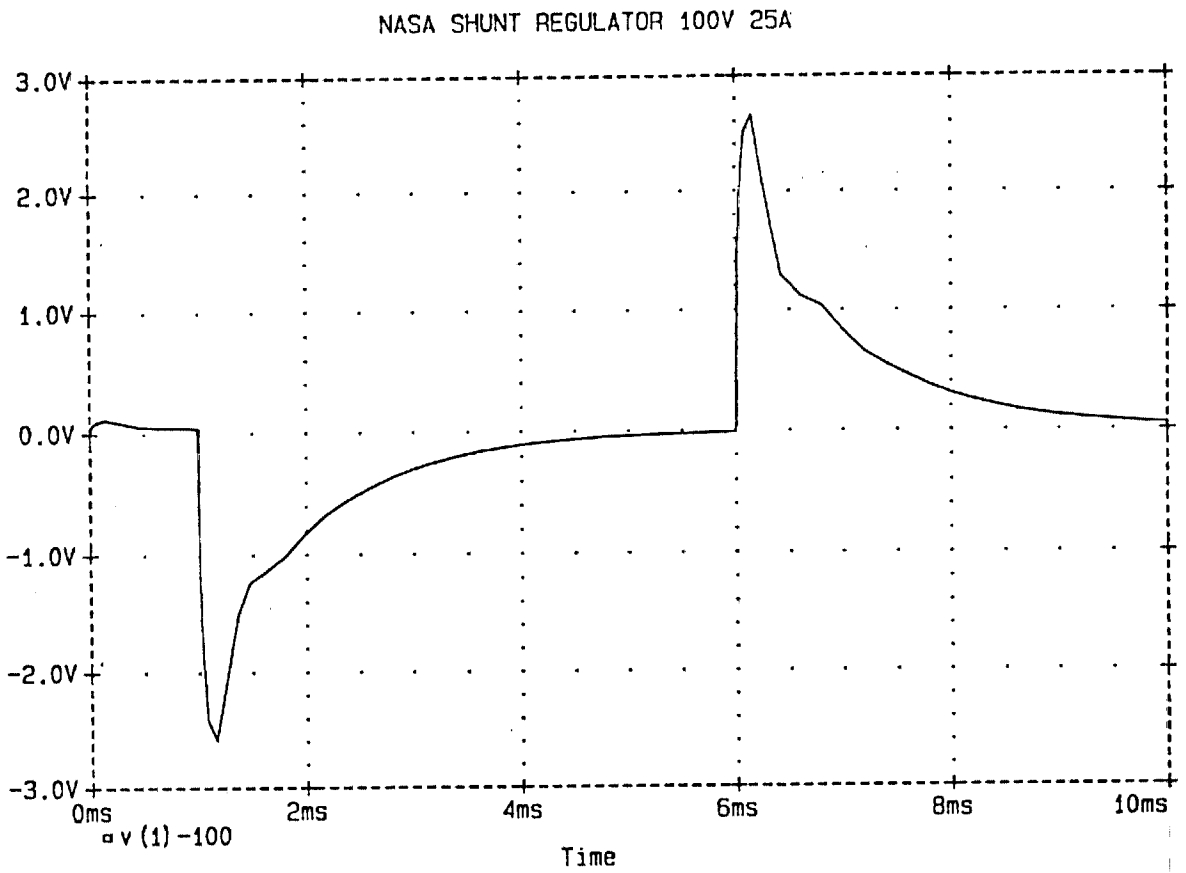


Fig. V-26. PSpice simulation of load step-change with $c_o = 380\mu F$. Shown is $v_o - 100$.

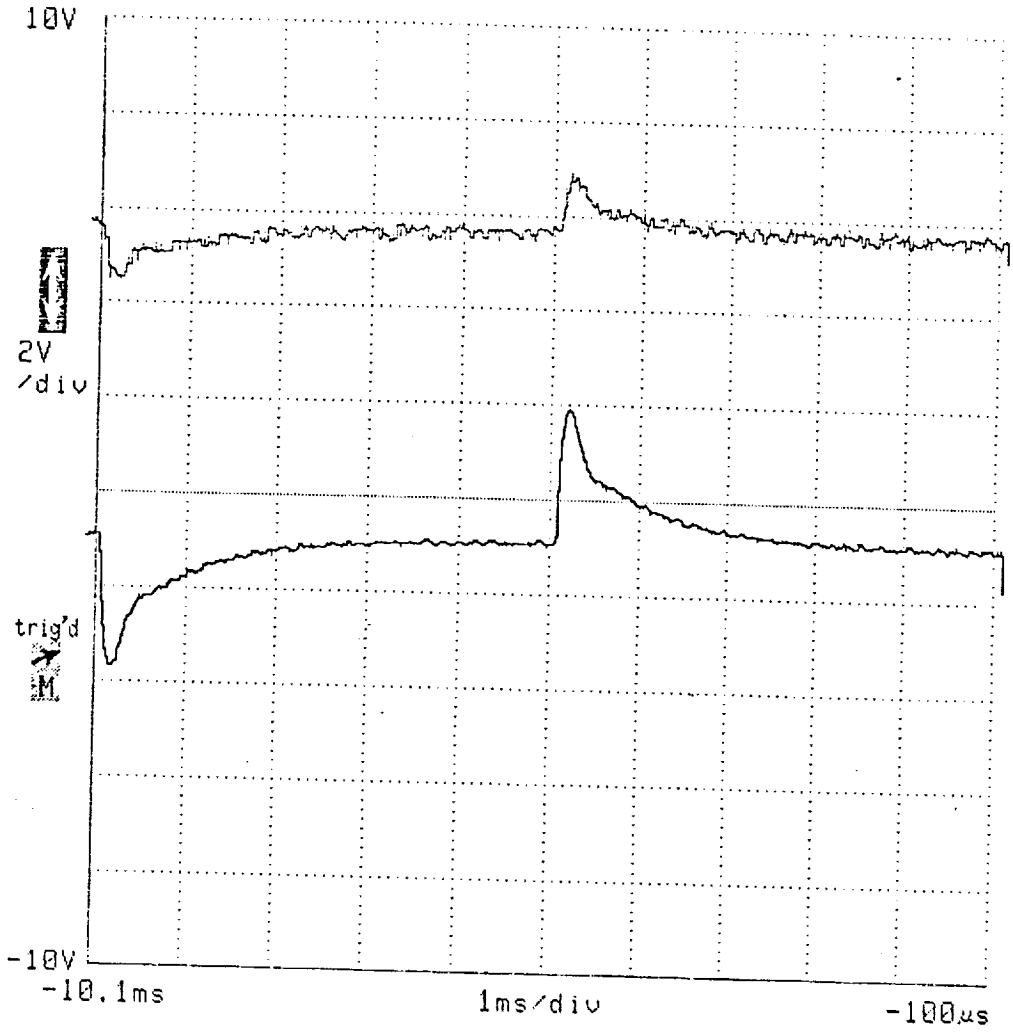


Fig. V-27. Experimental load step-change with c_o = 380µF. Upper: v_o - 100 at 5 V/div (unprocessed). Lower: v_o - 100 at 2 V/div. (event-averaged). Timebase: 1mS/div.

VI. THERMOELECTRIC CONVERTER SYSTEM PERFORMANCE

Introduction

The simulation and experimental data presented thus far have shown that the TEC-shunt regulator combination is a well-behaved, low impedance voltage source under the conditions studied. However, the results of exceeding the regulation range of the shunt regulator should be considered, because the system has a high (1 pu) internal resistance when the shunt regulator drops out. The typical load will be either a single dc-dc converter (with its own controller) or possibly a distributed system composed of many dc-dc converters. Because of the constant-power characteristics of such a load, which imply a negative incremental resistance, dropout of the shunt regulator might trigger bistable or unstable operation. For a similar system composed of a photovoltaic array, shunt regulator and dc-dc converter, possible bistable operation has been demonstrated [8]. This possibiliby was therefore investigated by simulation and experiment. The results reported here will also be published in [16].

TEC - Shunt Regulator

The TEC and shunt regulator of Figs. V-5 - V-7 were simulated using PSpice and the model of Fig. V-17. Because the quasi-static characteristics of the system were being examined, and the shunt regulator contains a proportional-integral controller, the regulator terminal voltage tracked the reference voltage exactly, except when the regulation range was exceeded due to an overload. When the shunt regulator drops out, the TEC terminal characteristics become that of a 2 pu voltage source with 1 pu internal resistance. It is convenient at this time to define the following base quantities for the purpose of normalization:

V_{BASE} ≡ one-half the TEC open-circuit voltage,

I_{BASE} ≡ one-half the TEC short-circuit current, and

R_{BASE} ≡ the TEC internal resistance.

The expected TEC terminal voltage and current at full-load are both 1 pu, if a maximum-power-transfer design is used. Fig. VI-1 displays the static i-v characteristics of the TEC-shunt regulator combination in normalized form. The

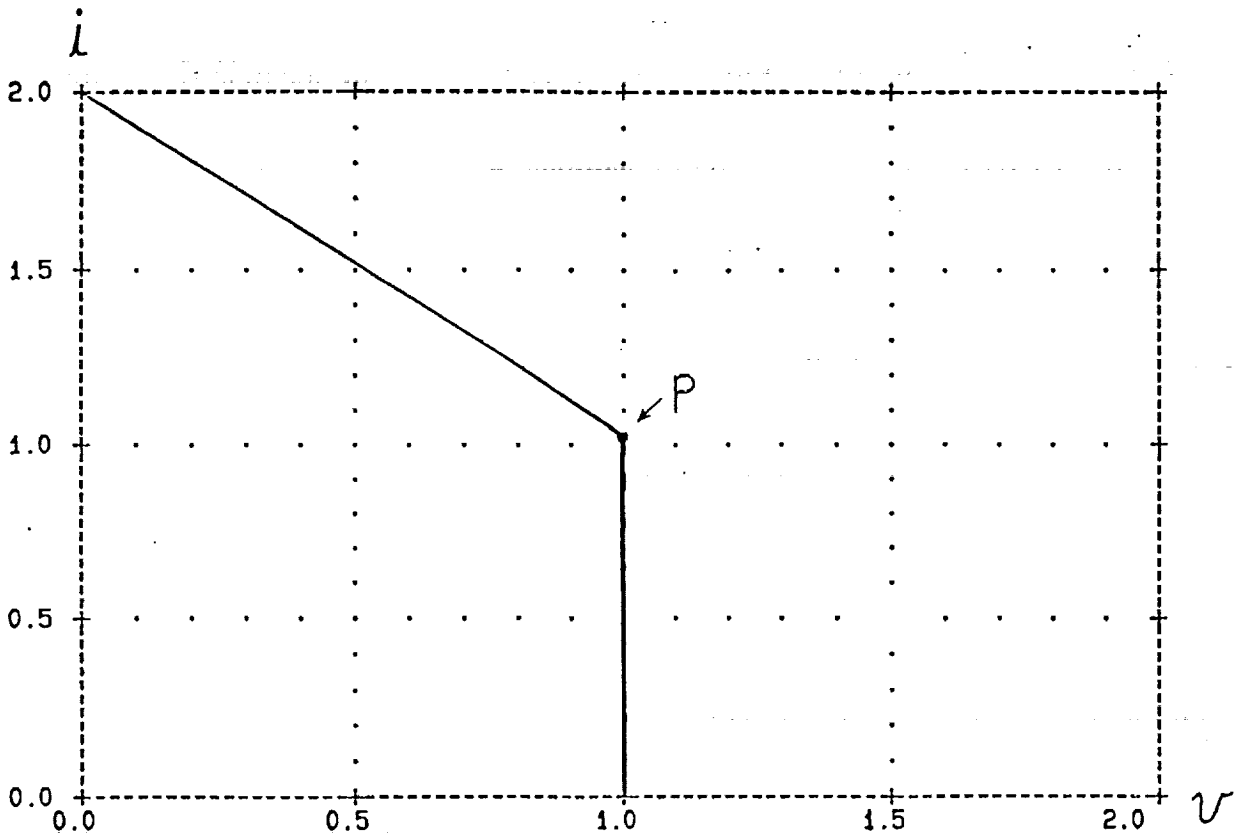
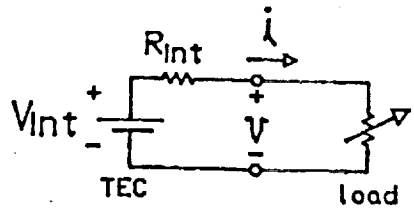
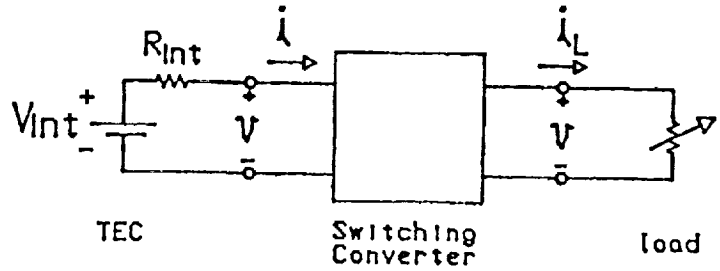


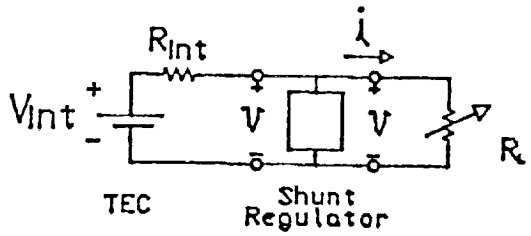
Fig. VI-1. Static i-v characteristics of TEC with shunt regulator.



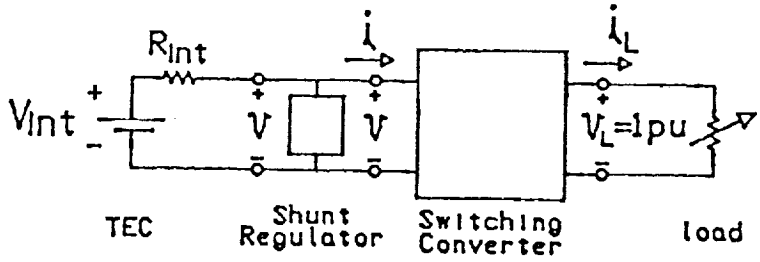
(a) Case 1



(b) Case 2



(c) Case 3



(d) Case 4

Fig. VI-2. Four cases: Thermoelectric converter with load and regulator.

design full-load operating point "P" is indicated in this figure.

Fig. VI-2 illustrates four possible systems configurations using a TEC. Case 1, Fig. VI-2 (a), shows the load connected directly to the TEC. In this case the load voltage v will vary over a 2:1 range as the load current varies from 0 pu to 1 pu. The resulting voltage regulation is not good, and the no-load TEC terminal voltage reaches 2 pu, unnecessarily stressing its internal insulation. Case 1 is therefore not considered useful.

Case 2, Fig. VI-2 (b), shows the addition of a switching converter, possibly to raise the TEC output voltage for transmission purposes. This switching converter could also be called on to provide load voltage regulation, but this would not reduce the voltage swings at the TEC output terminals. In addition to the TEC insulation, the converter's switching devices would also need to be rated for twice the full-load voltage stress. Therefore, this case is also considered unworkable.

Case 3, Fig. VI-2 (c), shows the addition of a shunt regulator to the TEC. The i-v characteristics of the TEC-shunt regulator combination are shown in Fig. VI-3 with several possible load characteristics superimposed. These are assumed to be resistive. The equilibrium point of the system is the point of intersection of the two characteristic curves. It can be seen that the system drops out of regulation for a load resistance less than 1 pu. At the rated-power-point P the shunt regulator is drawing no current; its presence does not reduce the efficiency of the system at full power, therefore. Case 3 represents a useful system, if the load characteristics are resistive. This is not likely to be the case, however, because many types of loads include internal switching converters (with regulators), which are best modeled as constant-power loads.

Case 4, Fig. VI-2 (d), is therefore considered next. The switching converter in this figure is assumed to have a regulated output voltage (v_L = 1 pu), with the restriction that it has both input and output current limiting set for 1.25 pu. The nominal input-voltage-to-output voltage conversion ratio is 1.0 in the following illustrations. However, the switching converter regulates by varying this conversion ratio (by varying the duty cycles of its switches): the upper bound for this conversion ratio N has been assumed to be 2.0, allowing for operation with a TEC degraded to an output voltage of 0.5 pu, and the lower bound for N has been assumed to be 0.1, perhaps due to a minimum duty cycle limitation. These

assumed conversion ratios are based on the choices of nominal input and output voltages; the converter illustrated here could therefore be implemented using either a buck or a boost configuration, with or without an internal transformer.

The characteristics of the model used for the switching converter are explored further in Fig. VI-4. Here the conversion ratio (N), the input current (i) and the load voltage (v_L) are plotted versus input voltage (v) for a load resistance of 1.25 pu. At very low input voltage the conversion ratio of the switching converter is limited to its maximum value, and the input characteristics are resistive. There is next a regime of input-current limiting, followed by output voltage regulation. These three regimes are indicated on Fig. V-4. It can be noted that output current limiting does not occur in this example, and that input current limiting is sometimes omitted from the switching converter design, in which case it would not appear here. The output voltage regulating (or output current limiting) regime is seen to be characterized by a negative incremental input resistance. It is well known that this complicates operation with a high-impedance source because of the posssibility of instability. However, it will be shown here that this negative-input-resistance characteristic also leads to three possible system equilibrium points, only one of which is desired.

Fig. VI-5 shows two sets of TEC-shunt regulator i-v characteristics, one for the nominal system, and another for a degraded TEC having a 25 percent reduction in its open-circuit voltage. Superimposed on these curves are the characteristics of the switching converter with two load resistances, 1.0 pu and 0.8 pu (an overload). The overload curve intersects the normal TEC-shunt regulator curve at a below-nominal voltage of 0.8, as expected. The full-load curve (R_L = 1.0 pu) intersects the normal TEC-shunt regulator curve in three places, however. Points A and C represent stable equilibrium points; point B is unstable. The desired operation point is C, but the design of the system should include preventing A, or returning to C if operation should inadvertantly shift to A.

Fig VI-5 suggests one possible mechanism by which operation could jump from the desired to an undesired equilibrium point. Assume that stable operation at C with R_L = 1.0 pu is interrupted by a momentary overload, corresponding to R_L = 0.8 pu. The operating point will rapidly jump to A, and remain there after the transient overload passes. A controller for the system must then intervene if

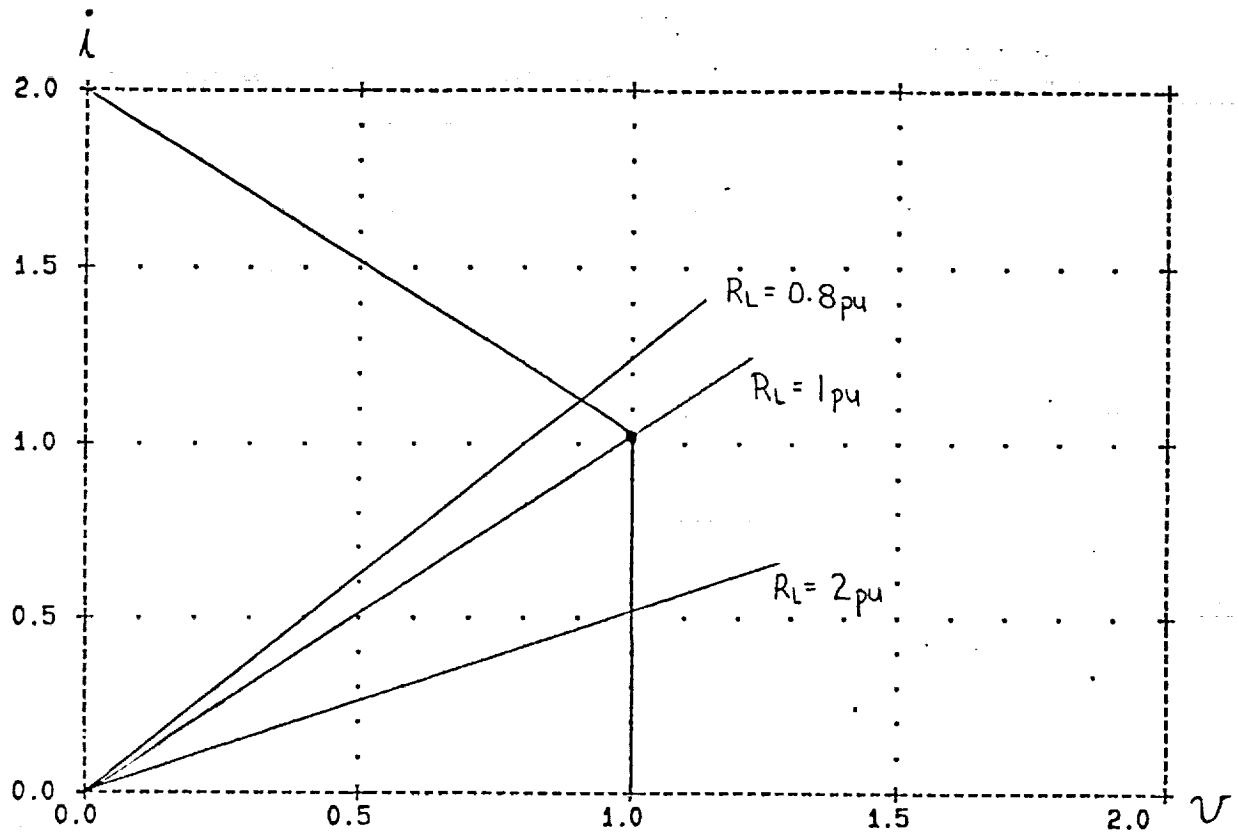


Fig. VI-3. TEC-shunt converter i-v characteristics with superimposed resistive load characteristics.

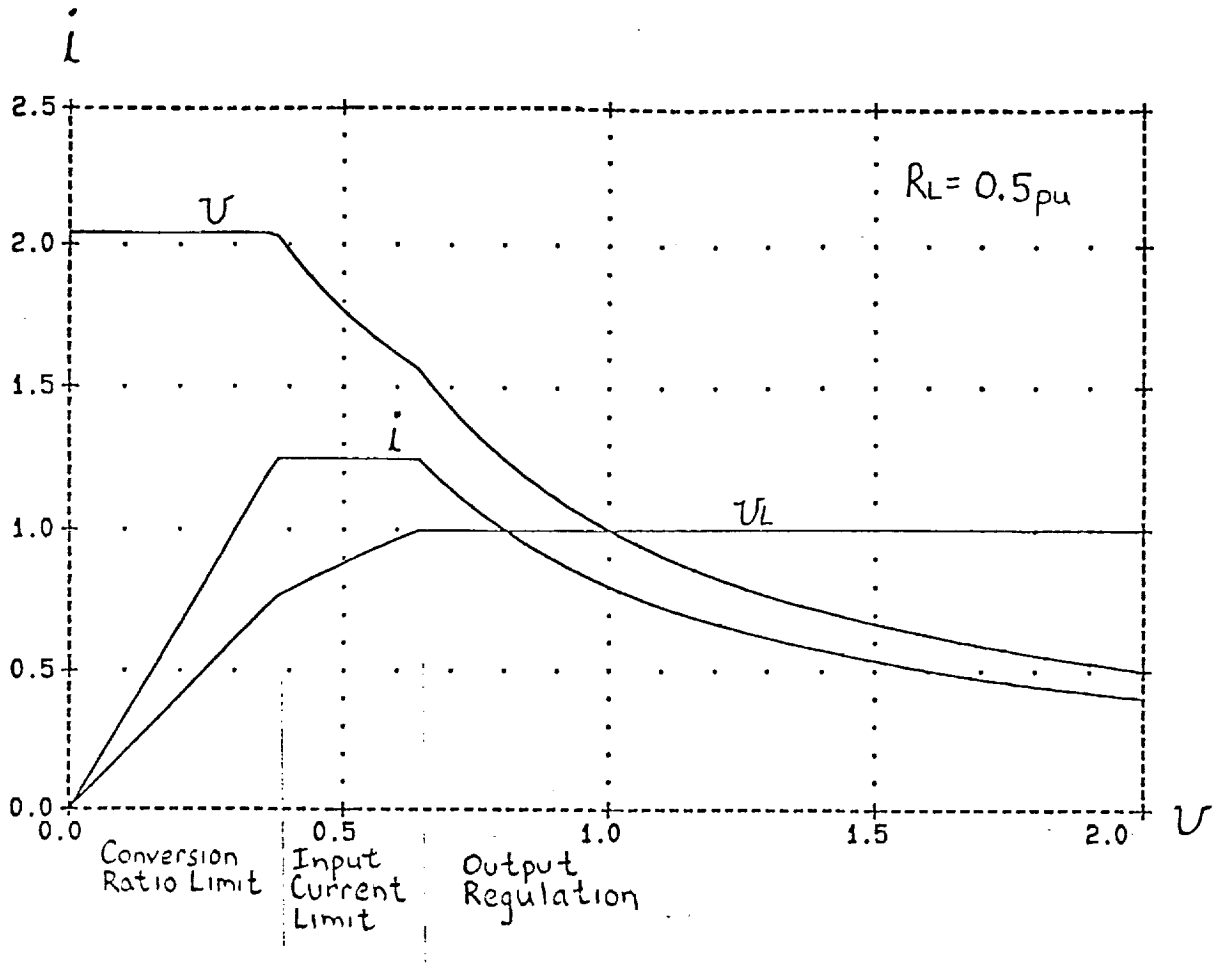


Fig. VI-4. Characteristics of the switching converter model. Conversion ratio (N), input current (i) and output voltage (vL) versus input voltage (v).

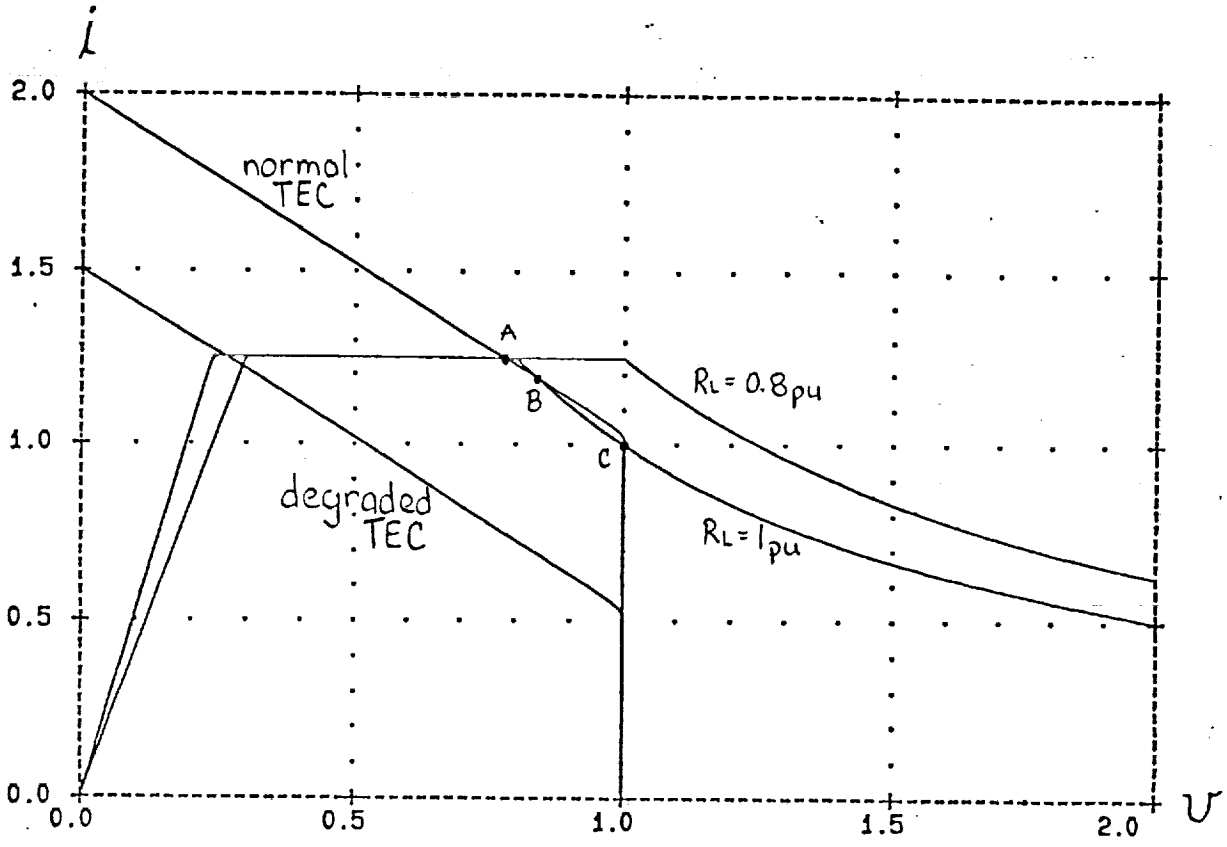


Fig. VI-5. Two possible TEC-shunt regulator I-V characteristics with two switching converter I-V curves (for R_L = 0.8 pu and 1.0 pu).

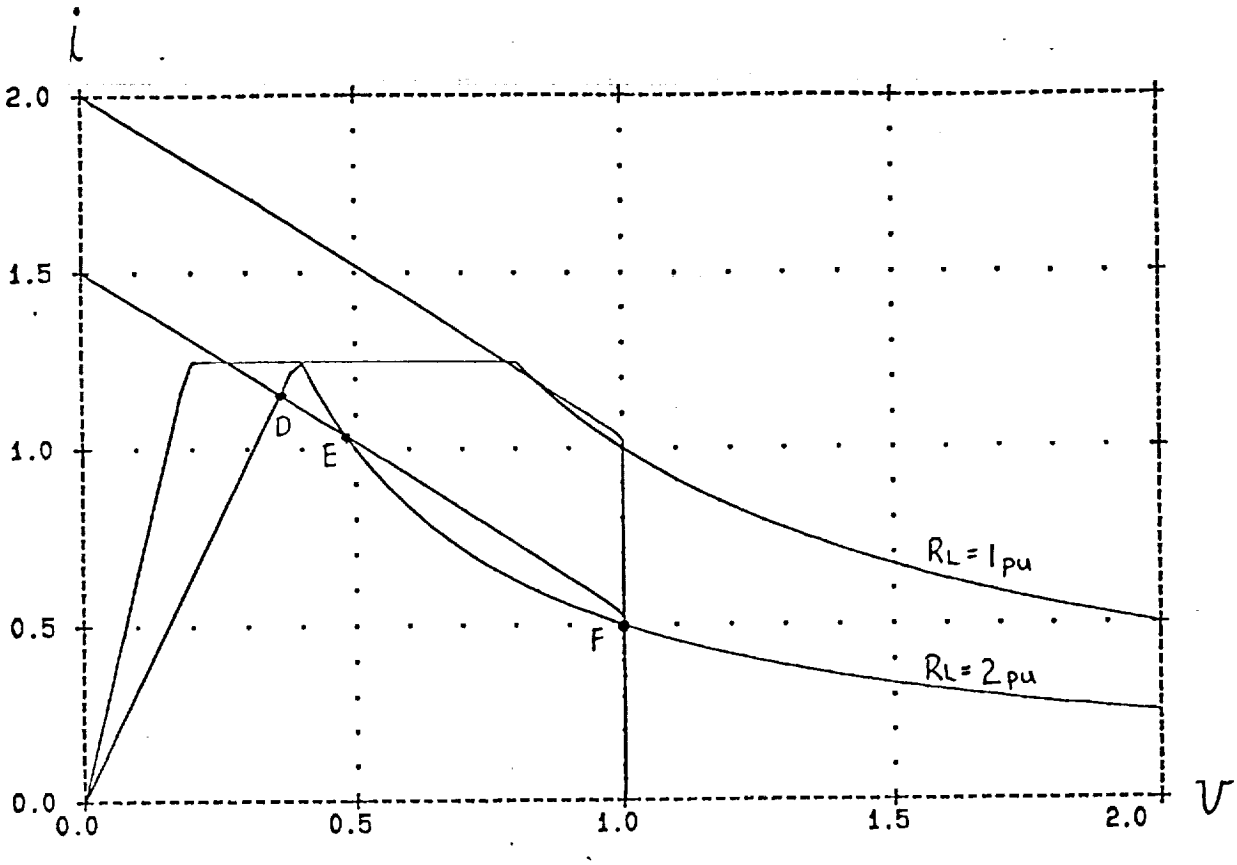


Fig. VI-6. Two TEC-shunt regulator IV curves with two switching regulator I-V curves (for R_L = 1.0 pu and 2.0 pu). Note that the maximum conversion ratio is 2.5 for this figure.

operation at C is to be re-established. Fig. VI-5 also suggests another much simpler solution: a slight reduction of the switching converter input current limit of 1.25 pu would eliminate points A and B in this illustration.

There are a number of interacting factors which determine the possibilities, however. Fig. VI-6 shows a case in which the maximum conversion ratio has been set to 2.5 (instead of 2.0). Load resistances of 1.0 and 2.0 pu are illustrated here. If derated operation with a degraded TEC is to be obtained, the conversion ratio should be wide enough to allow reduction in TEC voltage. In this figure, operation with a degraded TEC and reduced load is attempted, resulting again in two possible stable equilibrium points (D and F). Either a reduction of the input current limit, or of the maximum possible convertion ratio, would eliminate the undesired equilibrium points D and E in this example.

It is apparent that coordination of the current-limit settings and minimum/maximum duty-cycle limits in the switching converter with the i-v characteristics of the TEC can eliminate the undesired equilibrium points, if the TEC terminal characteristics are well defined. However, if the TEC i-v characteristics are subject to drift (e.g. degradation or start-up), it may be necessary to reprogram these settings throughout the life of the TEC.

Simulation Results

The possibility of two stable equilibrium points for the system of Fig. VI-2 (d) was demonstrated by means of a quasi-static PSpice simulation. The TEC and shunt regulator were modeled as indicated previously. The switching regulator was modeled as a variable-turns-ratio transformer with 100-percent power efficiency. A high-gain output voltage regulator was assumed, along with input- and output-current limiting at 1.25 pu. (Fig. VI-4 was generated by simulating this model.) A current load on the switching regulator was assumed to slowly ramp up, then down.

The results of this system simulation are shown in Fig. VI-7. The upper trace is a plot of switching converter output voltage v_L versus switching converter load current; the lower trace is a plot of the TEC terminal voltage v. Each variable was normalized using the base quantities given previously. It can be noted that

hysteresis "eyes" have appeared in this plot, the arrows indicating the traces corresponding to the upward and downward sides of the ramp. Fig. VI-7 reveals the presence of a disadvantageous operating mode in which the TEC terminal voltage is less than 1 pu, even though the load on the system is below rated. The unwanted mode was reached by having a momentary system overload, followed by a reduction in load current. This is not an unlikely event for many systems. As discussed previously, the location and extent of the hysteresis eye is a function of the switching converter input-current-limiter setting and conversion ratio restrictions, relative to the TEC terminal characteristics.

Experimental Results

The characteristics of the TEC system which were simulated were also verified experimentally. Because of limitations on the available dc power supply, the TEC was emulated by a 220 V supply in series with a 9.2Ω resistor, providing a maximum available power of 1315 W. The shunt regulator and switching regulator used were rated at 2500 W; however, the output current limit on the switching converter was reset to the 1315 W level. The characteristics of the TEC system are summarized in Table VI-1, along with appropriate normalization base quantities.

The circuit of Fig. VI-2 (d) was used. Fig. VI-8 is a plot of the normalized switching converter load and line voltages as the load current was cycled from 0 to 1 pu and back. The bistable behavior of the system is apparent. The appearance of Fig. VI-8 is somewhat difference from that of Fig. VI-7 due to the low efficiency of the switching converter, and the fact that it step-changed at the transitions between the two operating modes. (The measured efficiency in the desired mode was approximately 80-percent; in the undesired mode it increased to about 85-percent, representing in effect a change in the load current at the boundary points.) The simulation and experimental data do match qualitatively, and demonstrate the importance of including a provision in the system controller for dealing with this bistable phenomenon which would otherwise reduce the safely-available power.

Table VI-1. Experimental TEC-shunt regulator-switching converter specifications.

TEC Simulator	
Open circuit voltage	220V
Internal resistance	9.2Ω
Maximum power available	1315W
Shunt Regulator	
Voltage setting	110V
Maximum power	2500W
Switching frequency	20 kHz
Switching Converter	
Input voltage	110V
Output voltage	400V
Power rating	2500W
Normalization Base Quantities	
Voltage	110V
Current	12.0A
Resistance	9.2Ω

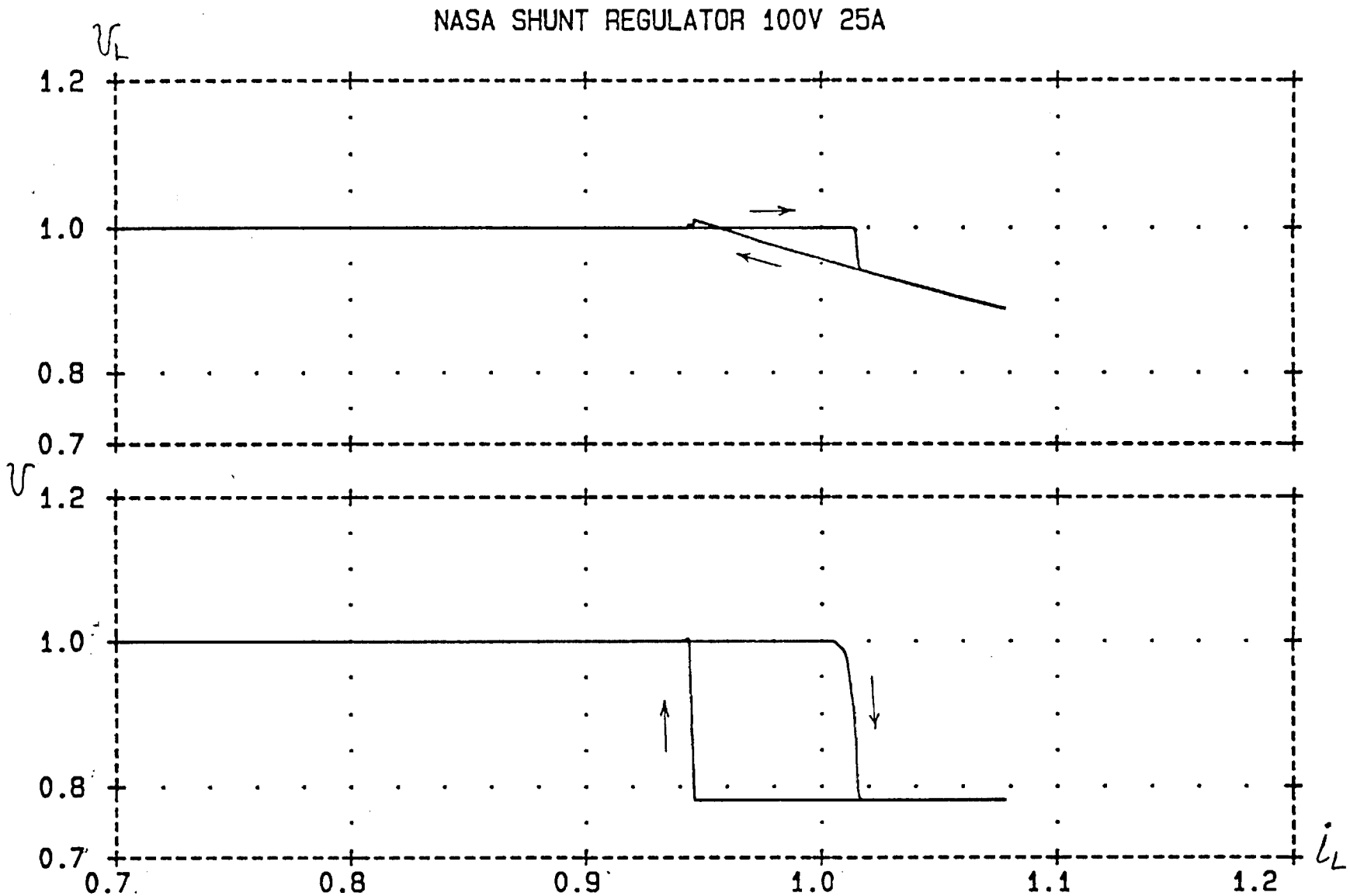


Fig. VI-7. Quasi-static simulation of TEC-shunt regulator-switching regulator system. Upper: Switching regulator load voltage vs. switching regulator load current. Lower: TEC terminal voltage vs. switching regulator load current. All plots are normalized.

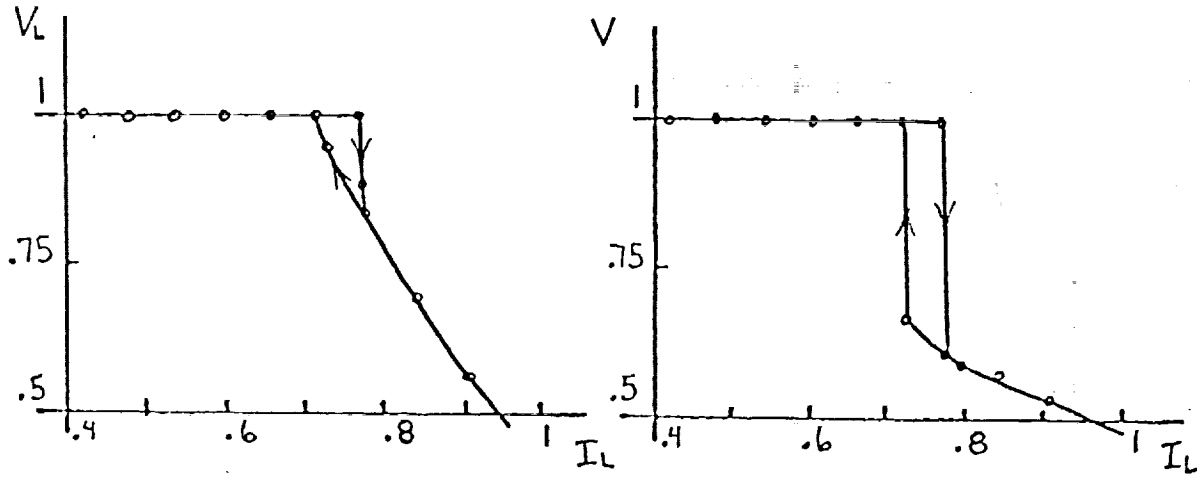


Fig. VI-8. Normalized experimental data. Switching converter load and input voltage versus load current.

VII. PHASE-CONTROLLED PARALLEL-LOADED RESONANT INVERTER

Introduction

The phase-controlled parallel-loaded resonant inverter (PC-PRI) has been proposed for use as a power processor in a 20 kHz sinusoidal-voltage power distribution system. Fig. VII-1 shows the power circuit of the 2.5-kW 20-kHz PC-PRI which was built as part of this experimental investigation. A suggested design procedure based on a fundamental-frequency phasor analysis was included in the last report on this grant [9] along with an exact closed-form steady-state solution. Experimental data taken in the steady state confirmed that the phasor analysis was a reasonable approximation. The suggested design procedure was also published in [15]. The experimental data agreed closely with the exact solution. However, the experimental inverter could not be operated at its rated input voltage, nor were any transient data taken.

Successful full-power operation of the PC-PRI has now been demonstrated. The load-short-circuit transient has been studied. This section of the report includes these additional results (with reference being made to [9]).

The Benefits of Resonant Power Conversion

Two salient benefits are usually attributed to resonant power conversion: lowering of electromagnetic interference (EMI) due to the inherent filtering action of the resonant tank, and improvement of the switching device i-v locus to lower switching losses. It should be noted that these benefits are obtained at the cost of increased switch conduction losses, due to the multiplied switch voltage and/or current. One of the basic decisions in the design of a resonant converter is the choice between zero-current switching and zero-voltage switching. In the case of the PC-PRI, below-resonance operation results in zero-current switching, if the load current is below some upper bound. Zero-current switching implies natural quenching of the current in the controlled devices, thus allowing the use of thyristors. Above-resonance operation results in zero-voltage switching, which implies natural quenching of the voltage across a blocking switch prior to turn-on of the controlled device. This permits the use of lossless snubbers.

The design procedure reported in [9, 15] showed that above-resonance design

of the PC-PRI requires substantially increased tank volt-ampere ratings. The experimental PC-PRI was therefore designed for below-resonance operation at 65- to 70-percent of the resonant frequency. The tank elements were chosen to guarantee zero-current switching for any load current having a magnitude below the full-load rating. Although natural quenching of the MOSFET current occurred, MOSFET turn-on caused a hard commutation of the antiparallel diode current. Because the initial design used the MOSFET's internal body-drain diodes, which had a lengthy reverse-recovery, this commutation was snubbed with substantial commutating inductance. This inductance then left the PC-PRI vulnerable to even a transient commutation reversal: any interruption of the current in the inductance resulted in a difficult-to-snub overvoltage spike. The PC PRI was therefore not considered fault-tolerant when operated at its design input voltage.

The solution implemented was the removal of the commutating inductors, leaving only an estimated 350 nH of stray inductance. The MOSFET body-drain diodes were blocked with a Schottky diode: Unitrode UES-2606 diodes were added in antiparallel to the Motorola MTM 40N20 MOSFETs. Each inverter switch in Fig. VII-1 was implemented using four paralleled MTM 40N20s and two paralleled UES 2606s (four paralleled sections). The overshoot voltage was controlled using a nonpolarized RC snubber (0.068μF and 1.67Ω).

The PC-PRI with fast antiparallel diodes was tested near its rated loading of 2500 VA with its rated dc input voltage of 100 V and found to be load-short-circuit tolerant. Operation with up to 120 Vdc was possible; the design value of 150 Vdc was not achieved due to the voltage overshoot caused by the 350 nH of stray inductance under short-circuit conditions. A lower-inductance circuit layout together with more-lossy snubbers would have extended the input voltage range. Because the steady-state solution presented previously [9] was well verified, the transient behavior of the updated experimental PC-PRI will be described next.

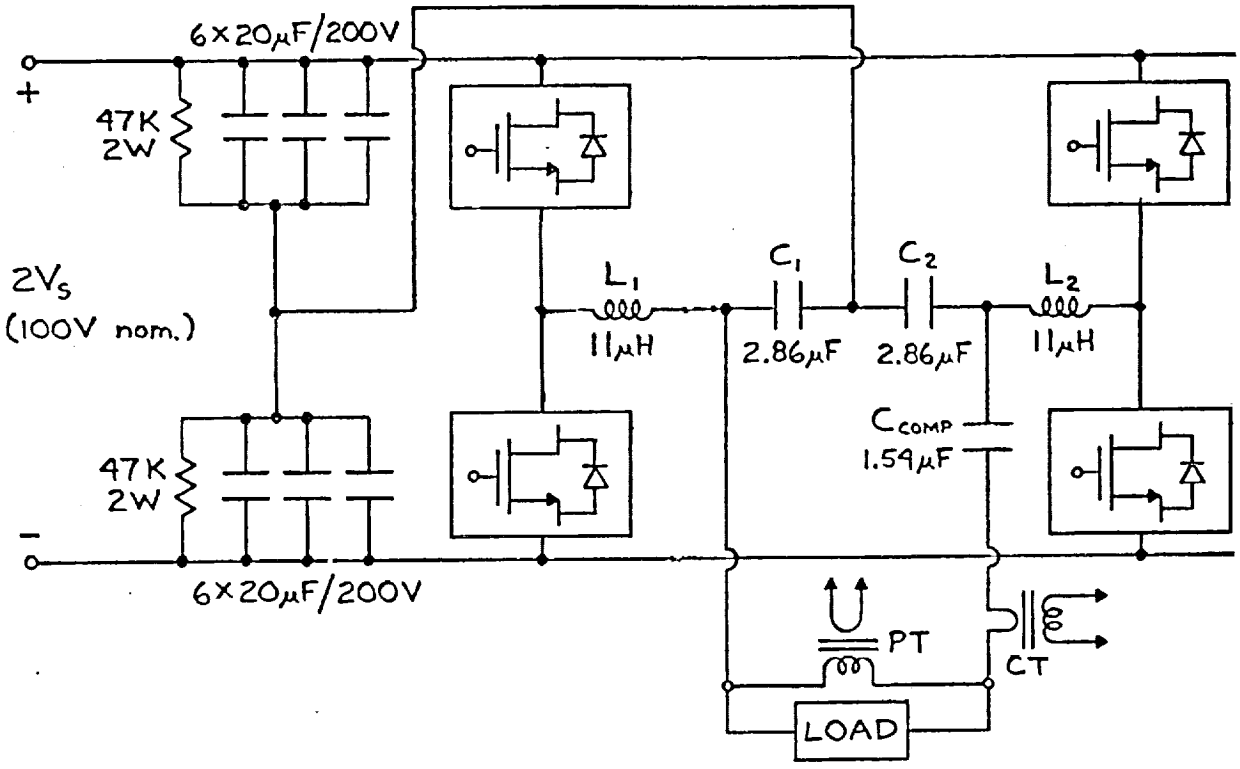


Fig. VII-1. Basic power circuit of phase-controlled parallel-loaded resonant converter.

Experimental Transient Behavior

Two experiments were performed: one was a switched load resistance, and the other a switched load-short-circuit. The experimental arrangement is shown in Fig. VII-2. A timing signal synchronous with the PC-PRI switching frequency was taken from the controller and fed to a divide-by-1000 counter. The output of the counter was used to trigger a Wavetek 801 pulse generator. The output pulse was used to control the MOSFET load switch. The pulse generator applied an adjustable trigger delay and an adjustable output pulse width, thus allowing the load switching to occur at an adjustable position in the inverter switching cycle, and to have an adjustable time duration. The divide-by-1000 counter allowed the load switching event to be repetitive at a low frequency (20 Hz), thus permitting display on a standard non-storage oscilloscope. The repetitive display of the switching transient with adjustable duration and positioning within a switching cycle was used to search for worst-case incidents. It was found that the transient results depended significantly on the positioning of turn-on and turn-off within the PC-PRI switching cycle.

The first set of data were taken with the original PC-PRI power circuit having commutating inductors [9] and a switched load resistance drawing slightly more than the design-full-load current corresponding to the dc input voltage being used. Fig. VII-3 displays the load voltage and current together with one of the inverter switch currents. It should be noted that the PC-PRI was being tested at one-half its rated voltage: the load voltage and current were therefore approximately 80 Vrms and 9 Arms. It can be seen in Fig. VII-3 that steady-state is reached both with the load switched on and off. Fig. VII-4(a) and VII-4(b) provide expanded views of Fig. VII-3 at turn-on and turn-off.

The commutation of one of the PC-PRI switches can be seen on the lower trace in Fig. VII-4(a). The negative switch current prior to turn-off indicates the expected zero-current-switching sequence. The antiparallel diode reverse-recovery current is also apparent at switch turn-off. It can be seen in this figure that the antiparallel diode conduction interval nearly disappears during the transient following application of the load. This would imply a commutation failure in a thyristor-based inverter. Fig. VII-4(b) provides a detailed view of Fig. VII-3 at turn-off of the load current. Interestingly, it can be noted that the peak

transient switch current occurs after load turn-off.

Load-short-circuit transient data were recorded for the PC-PRI of Fig. VII-1. The PC-PRI was operated at rated voltage (100 Vdc) with a resistive load drawing rated load current (14.5 Arms). The full-load voltage was 154 Vrms; the resulting loading was 2200 VA. The input conditions were 100 Vdc and 24.4 Adc; the power efficiency was 90-percent, based on the measured phase angle of the resistor bank (8 degrees). Fig. VII-5 shows the application and removal of a short circuit to the loaded converter. The circuit of Fig. VII-2 was used, except for the omission of the isolation transformer and the use of a 50 A/500 V Darlington transistor as the shorting switch. Fig. VII-5 shows a short-circuit current cresting at 150 A, with the somewhat sluggish response of the current limiter beginning after the fourth cycle of the fault. Figs. VII-6 and VII-7 show the current in L, and the voltage across switch S1 at three different times during the fault. The commutation conditions in the inverter can be deduced from these.

Fig. VII-6(a) was taken at the inception of the short circuit. The opening of S1 can be detected by the rising edge of v_{s1}; normal commutation requires diode current at this time, which implies a negative-signed current. Several cycles in which there is positive-signed current at switch opening can be seen, implying current interruption by the controlled switch. Fig. VII-6(b) was taken later during the load short-circuit. It can be seen here that the normal commutation sequence has been re-established. Fig. VII-7 shows the transient occurring at removal of the load short-circuit. In both Figs. VII-6 and VII-7 the modulation of the dc-side voltage by the flow of large fault currents through the bypass capacitors (and layout inductance) can be seen.

Discussion

The PC-PRI requires many of the design considerations common to all voltage-sourced topologies; however, the diode-to-gated-switch commutation was found to be particularly troublesome in the experimental hardware. This commutation was improved by using the fastest available antiparallel diodes. A snubbing inductor can be added to lower the diode reverse-recovery current while extending the charge-recovery time; however, this inductor interfers with gated

turn-off of the controlled switch. Present voltage-sourced-inverter design practice minimizes the stray inductance while tolerating increased peak currents (and switching losses). This is a good approach in a voltage-sourced inverter called on to make "hard" commutations in both the diode-to-switch and switch-to-diode sequences. However, the PC-PRI eliminates one set of hard commutations in the steady state, which should permit the use of large snubbers optimized to ease the other set of commutations. This was found to be a good design approach based on steady-state operation only, yet it renders the PC-PRI vulnerable to damage in the event of load short-circuit.

The experimental photos show that reversed commutation on a transient basis is a real possibility. The possibility of a reversed commutation sequence was handled in the experimental inverter by avoiding the use of substantial snubbers, and by providing fast antiparallel diodes. Unfortunately, this abandons one of the benefits of resonant power conversion: to ability to use slow diodes. For the PC-PRI there are at least two additional solutions, including above-resonance operation and a controller which detects and prevents an impending reversed commutation. Above-resonance operation will probably be ruled out due to the high tank volt-ampere ratings that would be required. The use of additional controller hardware will probably be mandatory in a high-power design, for which the luxury of fast switching devices is not so readily available. In any case, it is recommended that the experimental setup of Fig. VII-2 be used to verify the fault-tolerance of any hardware built. It is important to keep in mind that timing of the fault within an inverter switching cycle can have some influence on the results, and that a lower-power inverter can easily have some tolerance for reversed commutations, while a full-scale inverter might not. The circuit of Fig. VII-2 permits an exhaustive search for the worst-case results of a fault in a convenient manner.

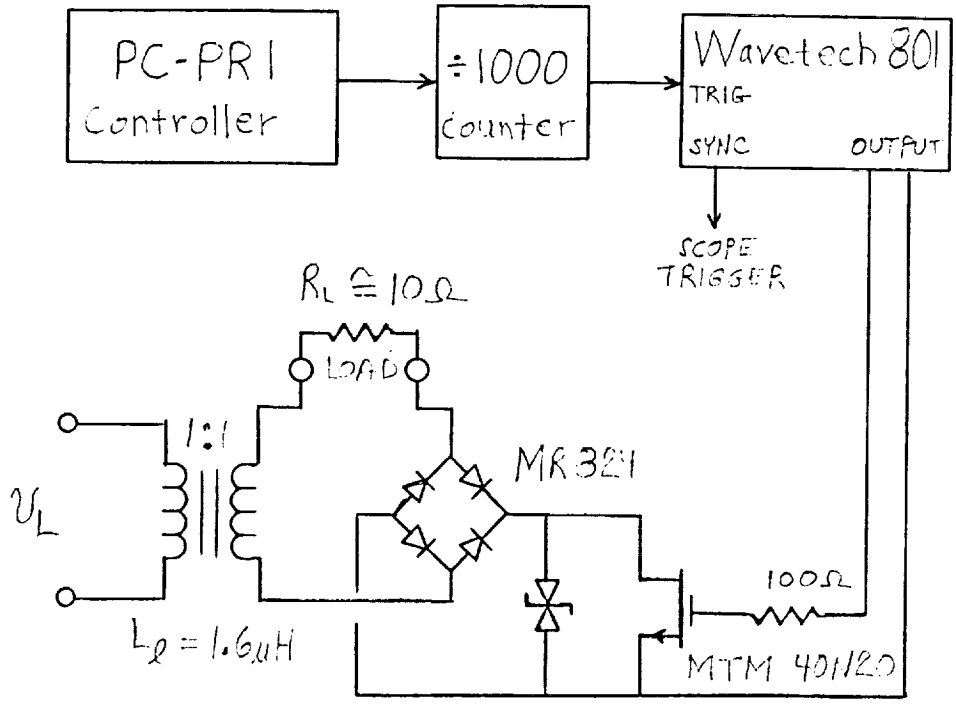


Fig. VII-2. Experimental arrangement for switched-load testing.

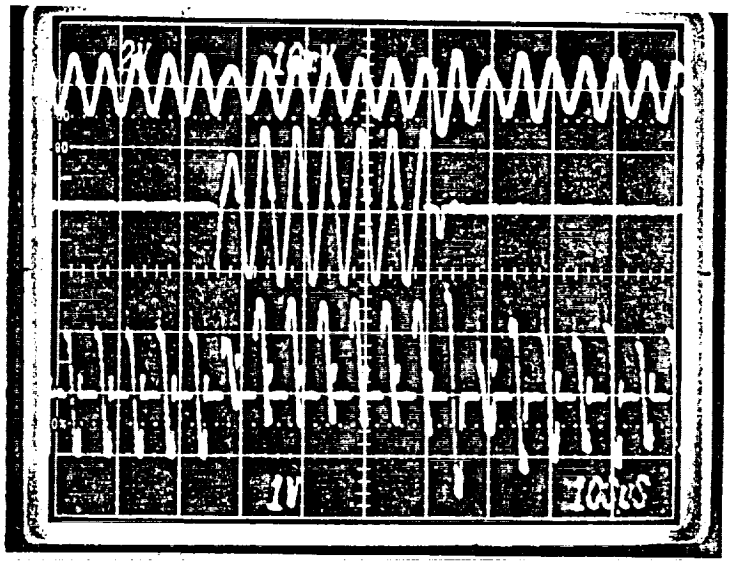


Fig. VII-3. Switched resistive load. Upper: Load voltage at 300 V/div. Middle: Load current at 10 A/div. Lower: Inverter switch current at 20 A/div. Timebase: 100 μs/div.

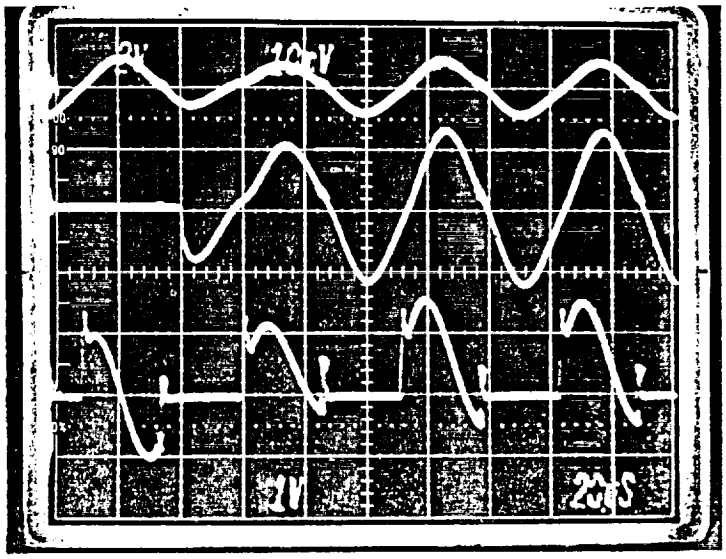


Fig. VII-4(a). Detail of Fig. -3. Timebase: 20 μs/div.

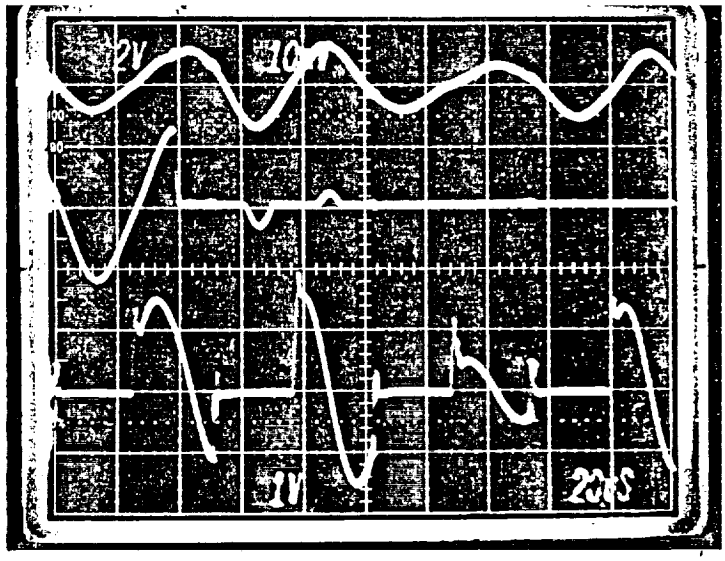


Fig. VII-4(b). Detail of Fig. -3. Timebase: 20 μs/div.

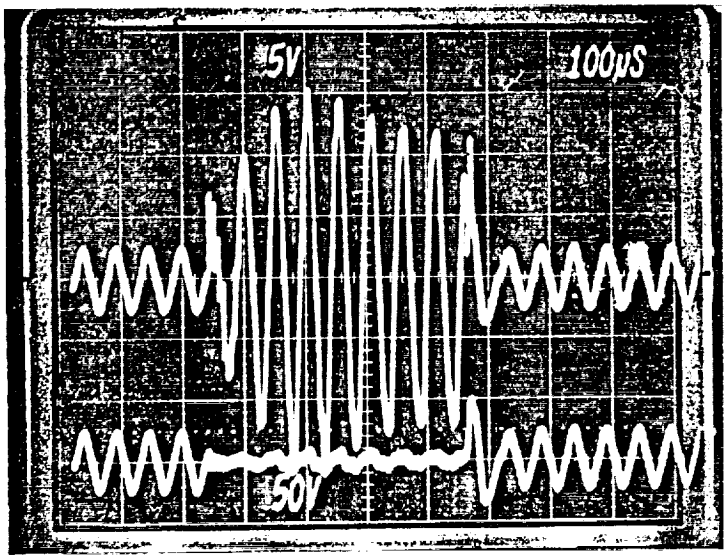


Fig. VII-5. Short-circuit transient, PC-PRI fully loaded. Upper: Load current at 50 A/div. Lower: Load voltage at 500 V/div. Timebase: 100 μs/div.

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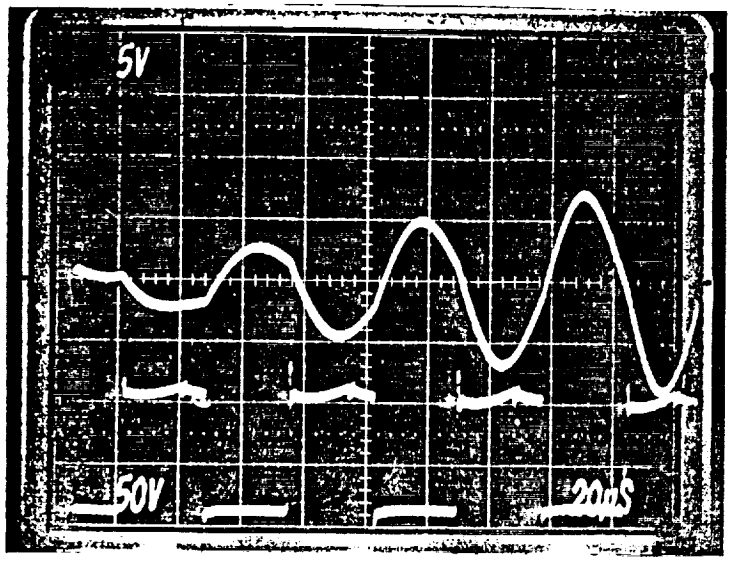

Fig. VII-6(a). Current in L_1, voltage on S1 at beginning of load short-circuit. Upper: Inductor current i_1 at 100 A/div. Lower: Switch voltage v_{s1} at 50 V/div. Timebase: 20 μs/div.

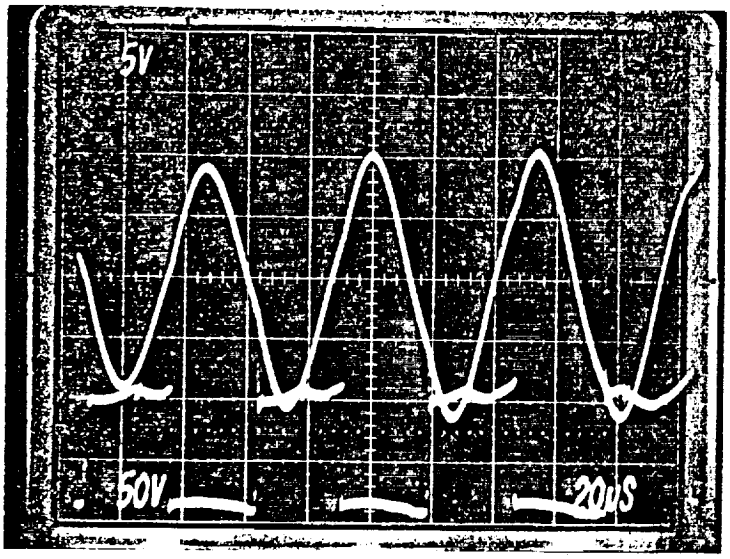

Fig. VII-6(b). Current in L_1, voltage on S1 as load fault curent levels off. Upper: Inductor current i_1 at 100 A/div. Lower: Switch voltage v_{s1} at 50 V/div. Timebase: 20 μs/div.

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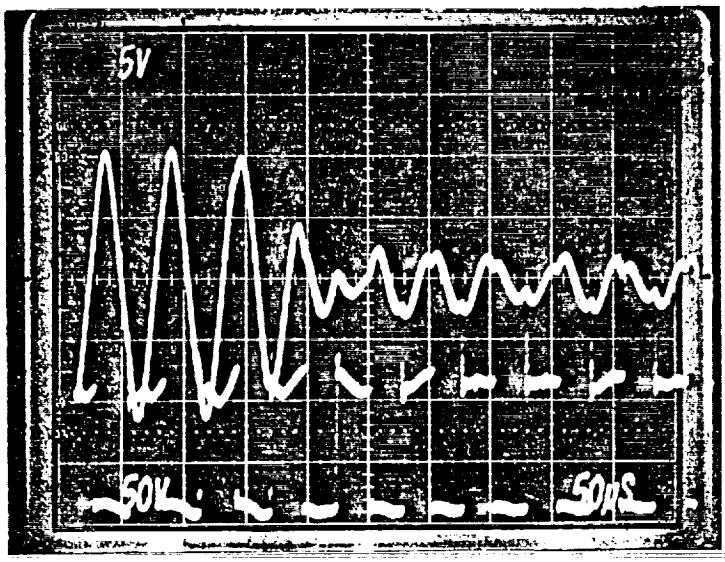

Fig. VII-7. Current in L_1, voltage on S1 at removal of load short-circuit. Upper: Inductor current i_1 at 100 A/div. Lower: Switch voltage v_{s1} at 50 V/div. Timebase: 50 μs/div.

VIII. SUMMARY

As described in the Introduction, the first goal of this project was to investigate various converters that would be suitable for processing electric power derived from a nuclear reactor. Fig. I-1 indicates the implementation of a 20 kHz system that includes a source converter, a ballast converter, and a fixed frequency converter for generating the 20 kHz output. This system can be converted to dc simply by removing the fixed frequency converter. Since a 2.5 kW version of the fixed frequency converter was developed as part of a previous project [9], this present study emphasized the design and testing of the source and ballast converters. A push-pull current-fed (PPCF) design was selected for the source converter, and a 2.7 kW version of this was implemented using three 900 watt modules in parallel. The steady state operation of this circuit has been analyzed extensively in previous references [2-4], but no references could be found on the open loop transfer functions. Since this information is needed to properly stabilize the converter, it was necessary to derive these functions for both the voltage and current regulation loops. Another problem that does not seem to have appeared in the technical literature is the stability analysis of parallel converters. The characteristic equation for two converters in parallel was derived, but this analysis did not yield any experimental methods for measuring relative stability. The three source modules were first tested individually and then in parallel as a 2.7 kW system. All tests proved to be satisfactory; the system was stable; efficiency and regulation were acceptable; and the system was fault tolerant.

The design of a ballast-load converter, which was operated as a shunt regulator, was investigated. The proposed power circuit is suitable for use with BJTs because proportional base drive is easily implemented. A control circuit which minimizes switching frequency ripple and automatically bypasses a faulty shunt section was developed. A nonlinear state-space-averaged model of the shunt regulator was developed and shown to produce an accurate incremental (small-signal) dynamic model, even though the usual state-space-averaging assumptions were not met. The nonlinear model was also shown to be useful for large-signal dynamic simulation using PSpice. Experimental data were presented confirming the automatic redundancy feature, and the large-and small

signal simulation results. Operation at 2500 W with a 120°C baseplate temperature (for the switching devices) was demonstrated.

Also investigated was the interaction of the TEC, shunt regulator and source converter when operated as a system. Both simulation and experiment showed that the system was potentially bistable. A momentary overload on the source converter could trigger a stable mode in which less-than-rated power was drawn, but the shunt regulator was out of regulation. This undesirable mode of operation can be prevented by providing an input current limiter on the source converter, with its setting coordinated with the TEC characteristics.

Final development and testing of the 2500 W phase-controlled parallel-loaded resonant inverter described in the previous report [9.] under this grant was completed. The validity of the proposed design procedure was confirmed for the steady state. Load-fault-tolerant operation was obtained in the laboratory inverter, but this required a snubberless design which gave up one of the benefits normally associated with resonant power conversion: the use of slow antiparallel diodes. A testing procedure for systematically verifying the transient short-circuit behavior of the inverter was demonstrated. It is proposed that this be used to verify any future inverter modifications intended to provide fault tolerance.

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